Remote Side-Channel Attacks on Heterogeneous SoC

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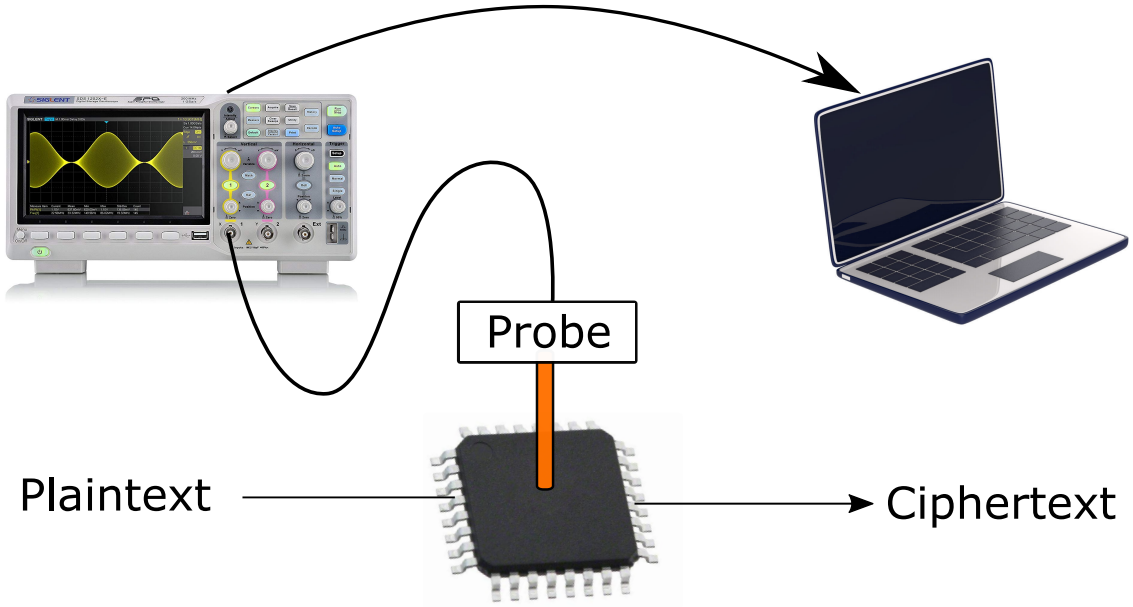
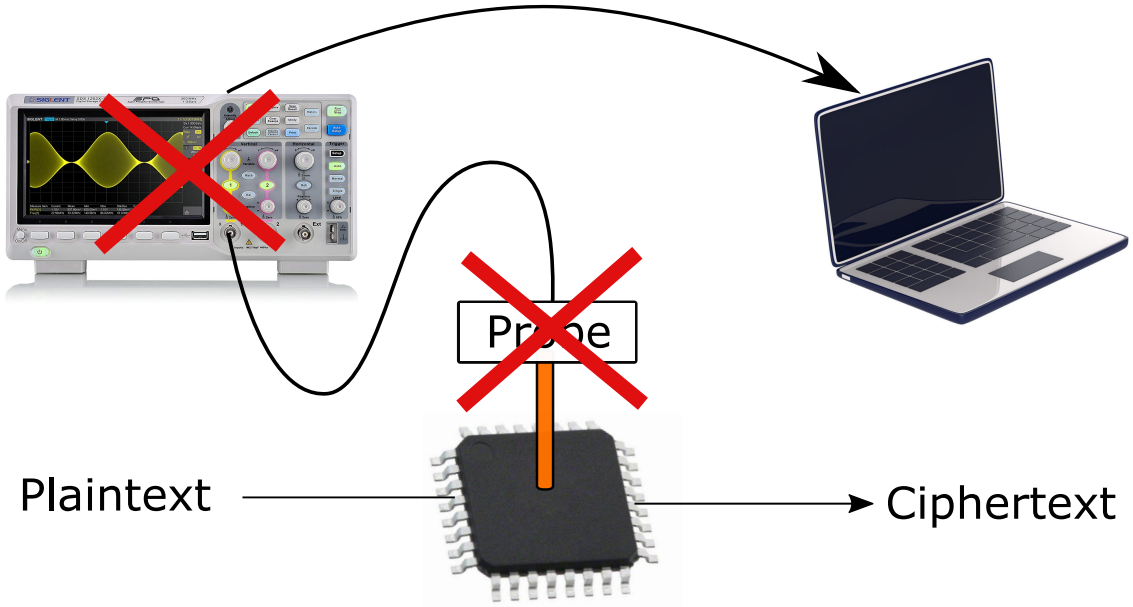
November 2019

- Type: fault injection attack (FIA) & side-channel attack (SCA).
- Target: smart cards, microcontrollers, system on chip...
- Means: oscilloscope, laser, EM probe...
- Range: **local**, direct physical access required.



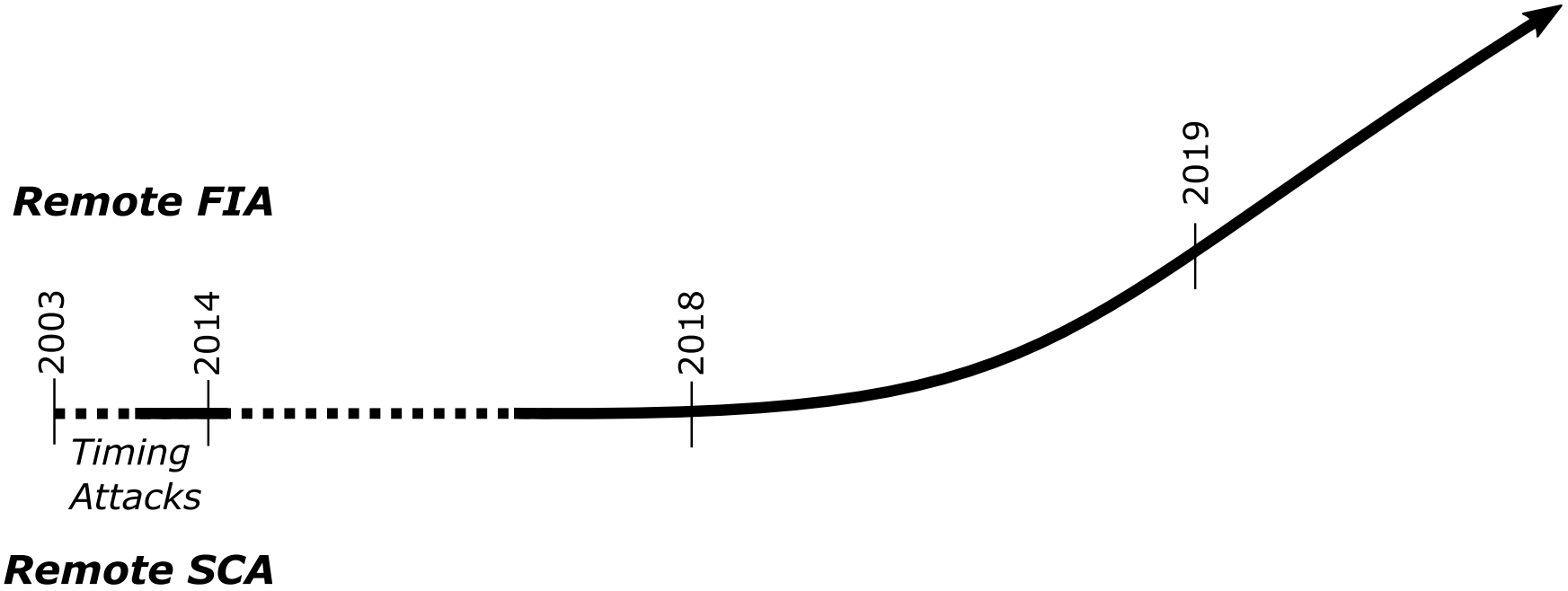
- Type: fault injection attack (FIA) & side-channel attack (SCA).
- Range: **remote, access to a network required.**
- Target: connected devices (IoT), data centers...
- Means: **resources available within the target**.



About remote hardware attacks

A temporal overview

- Remote hardware attack topic keeps on gaining in popularity:
  - Emergence of cloud services, IoT, decentralized computing



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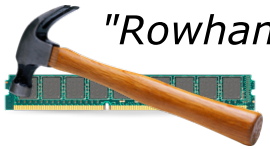
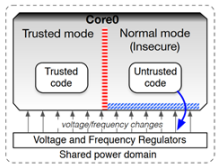


"Rowhammer"

Remote FIA



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2003 2014 2018 2019

Timing Attacks

Remote SCA

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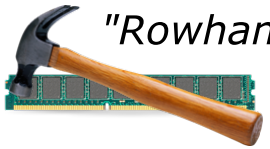

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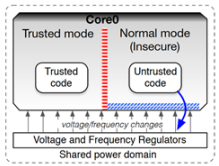

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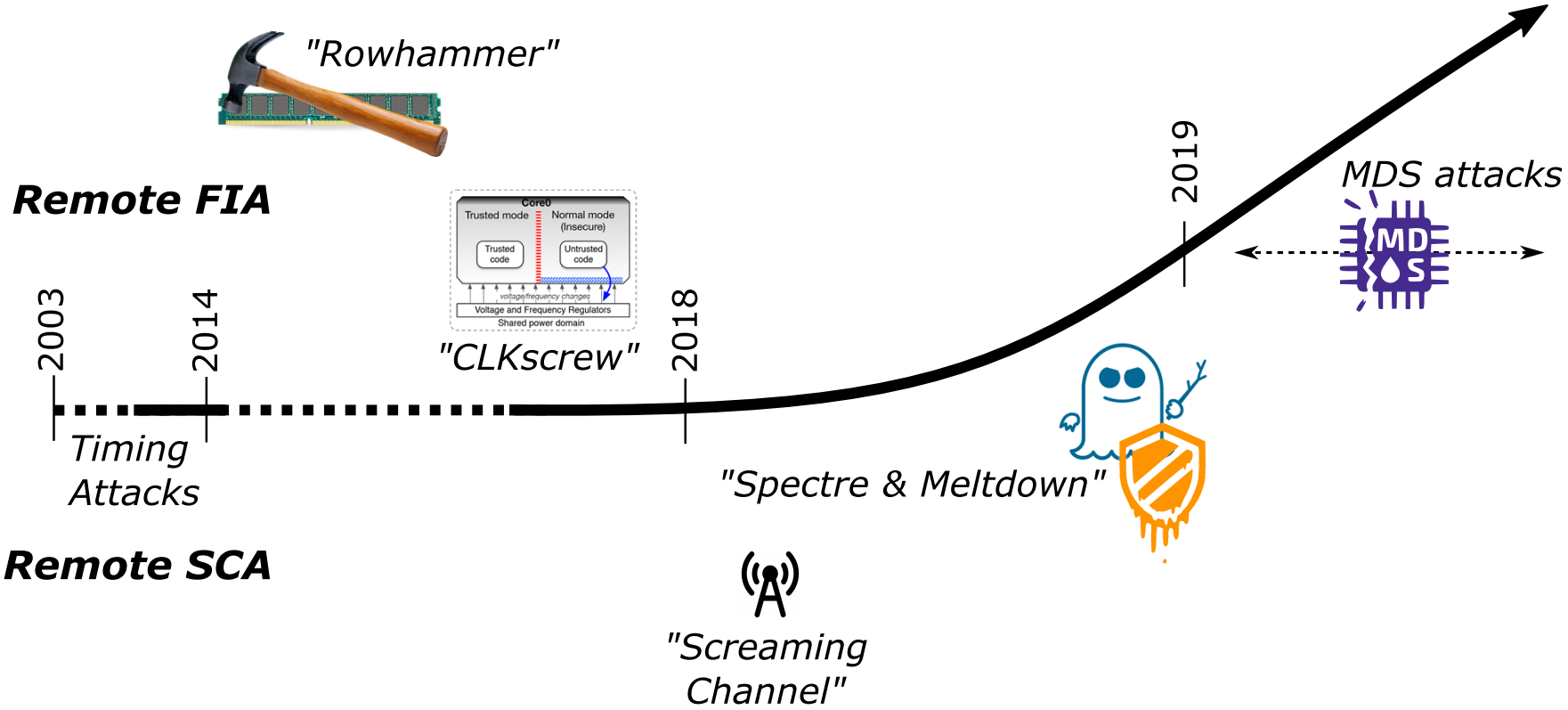

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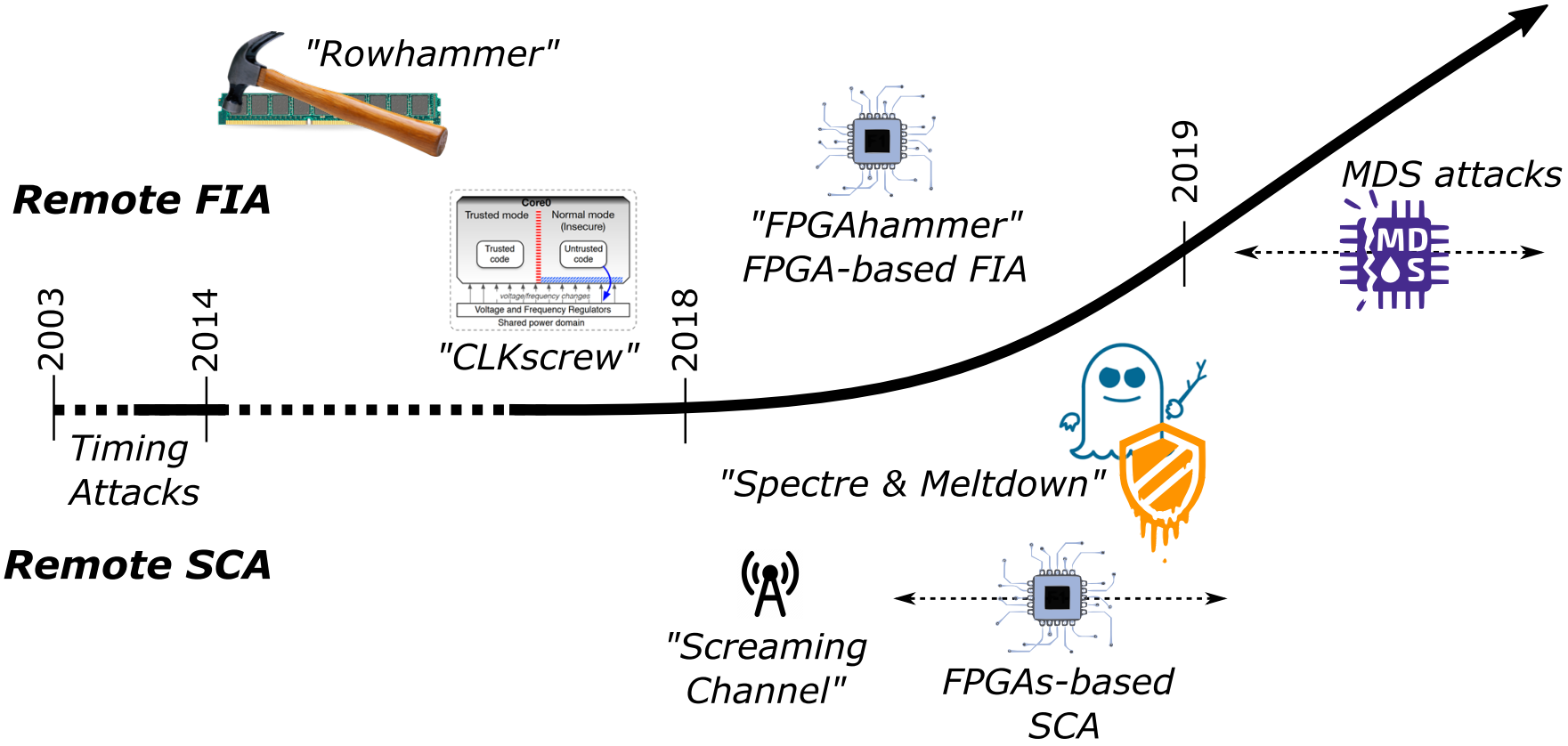

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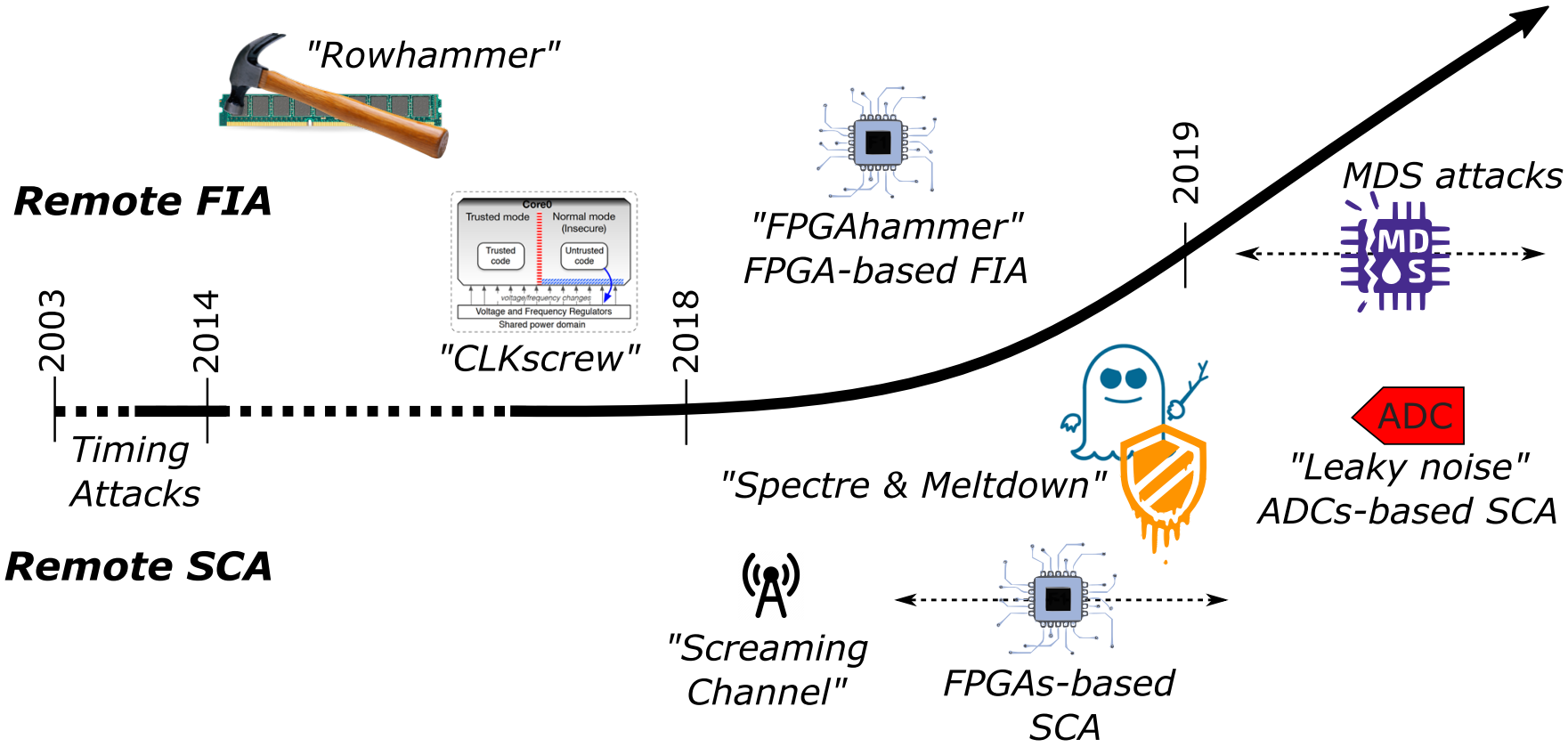

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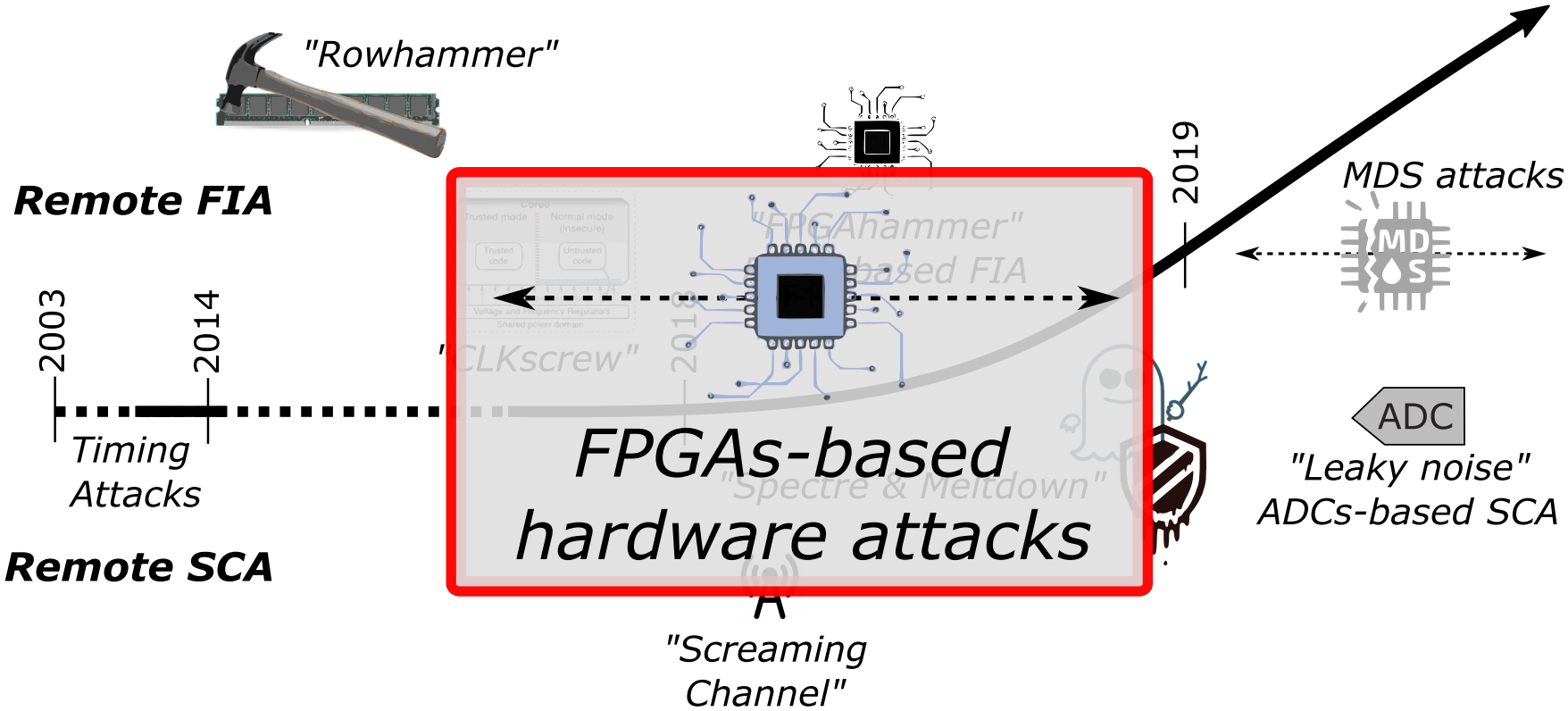

- Usual hardware attacks can be entirely reproduced within FPGA logic:
  - Encryption **algorithm** implementation.
  - Voltage glitch **injector** implementation (Krautter et al).
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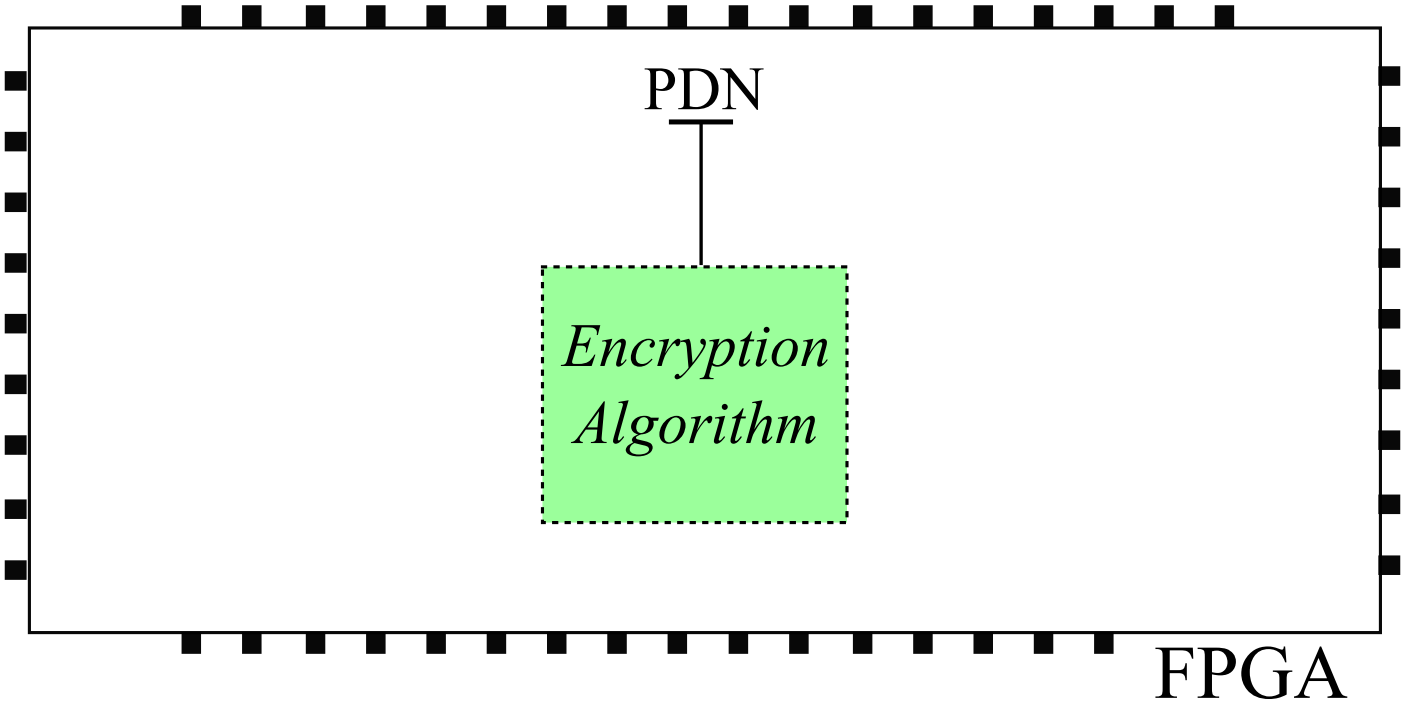

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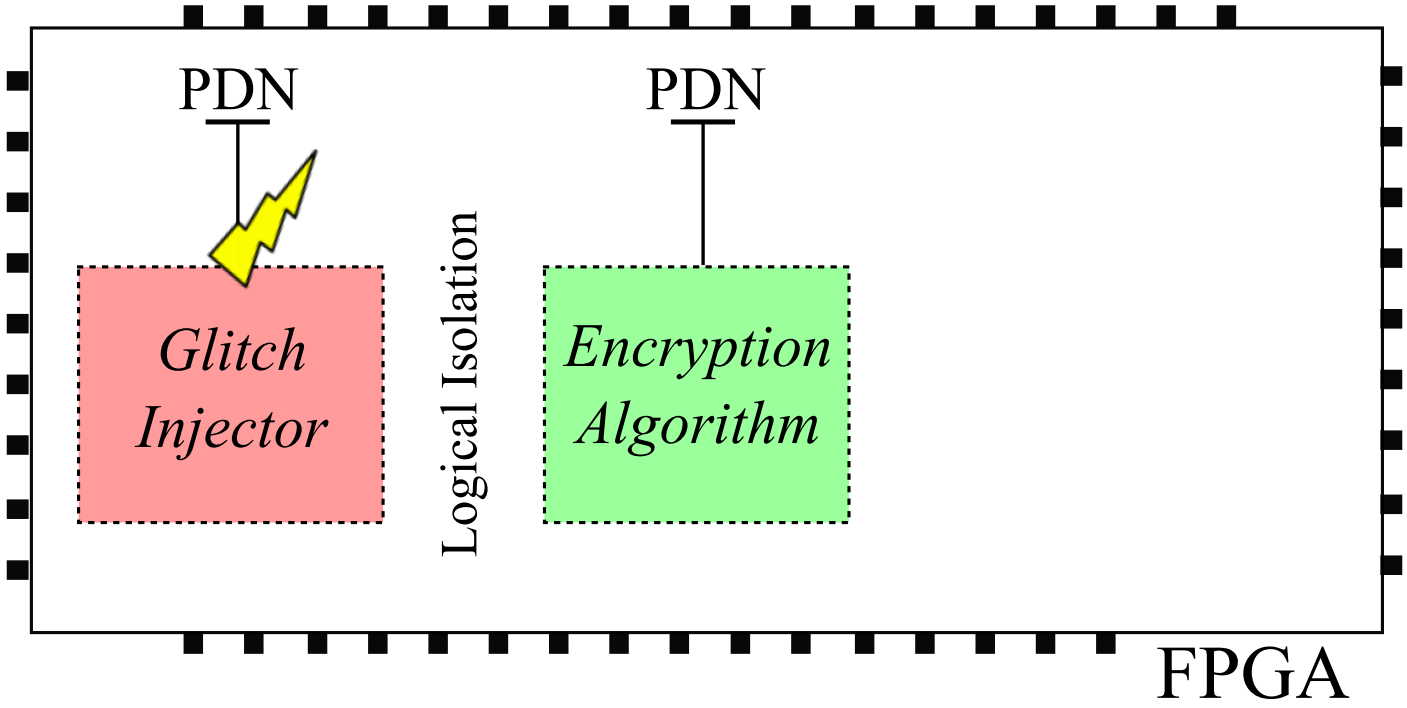

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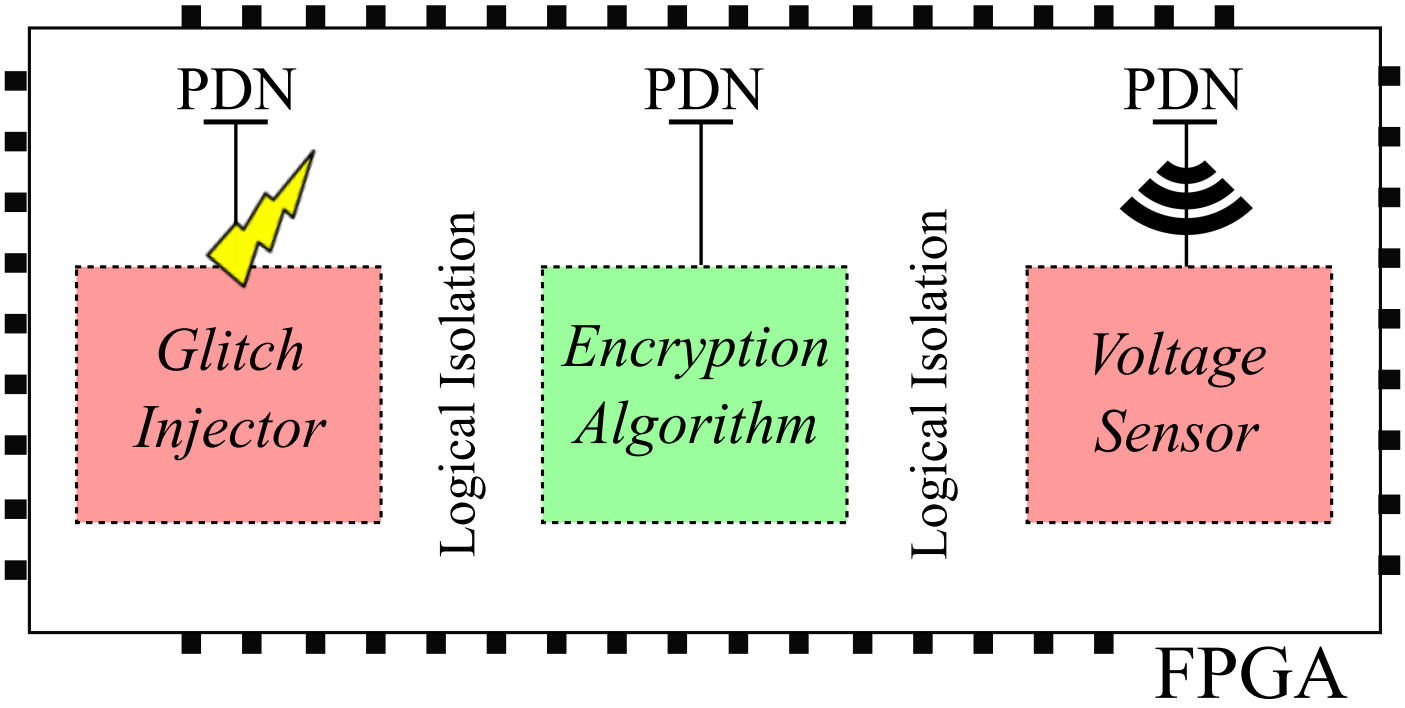
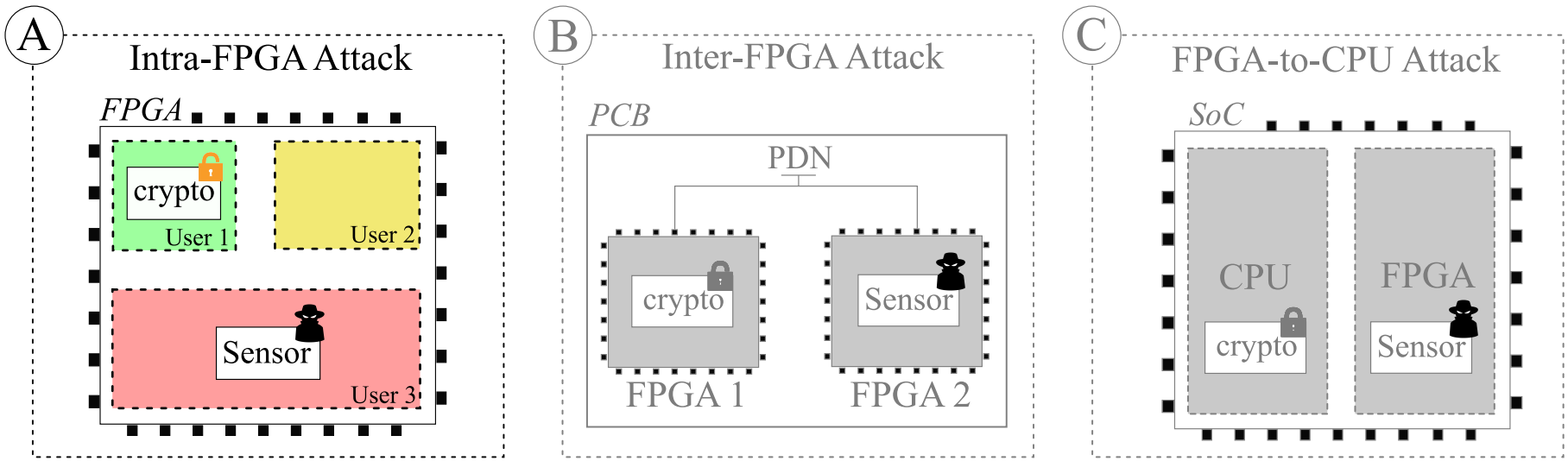


- Target: connected devices that embeds FPGAs.
  - (A) Multi-user FPGAs in **cloud datacenters** (Schellenberg et al).
  - (B) Printed circuit boards **PCB** (Schellenberg et al).
  - (C) **Heterogeneous** connected **SoCs** (Zhao et al).



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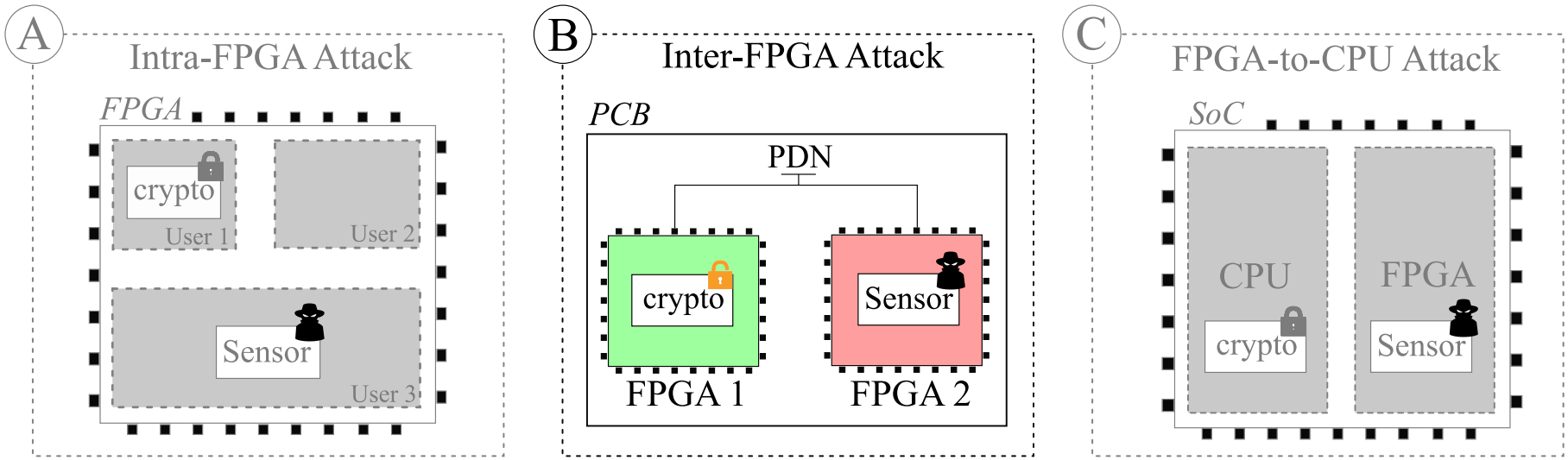

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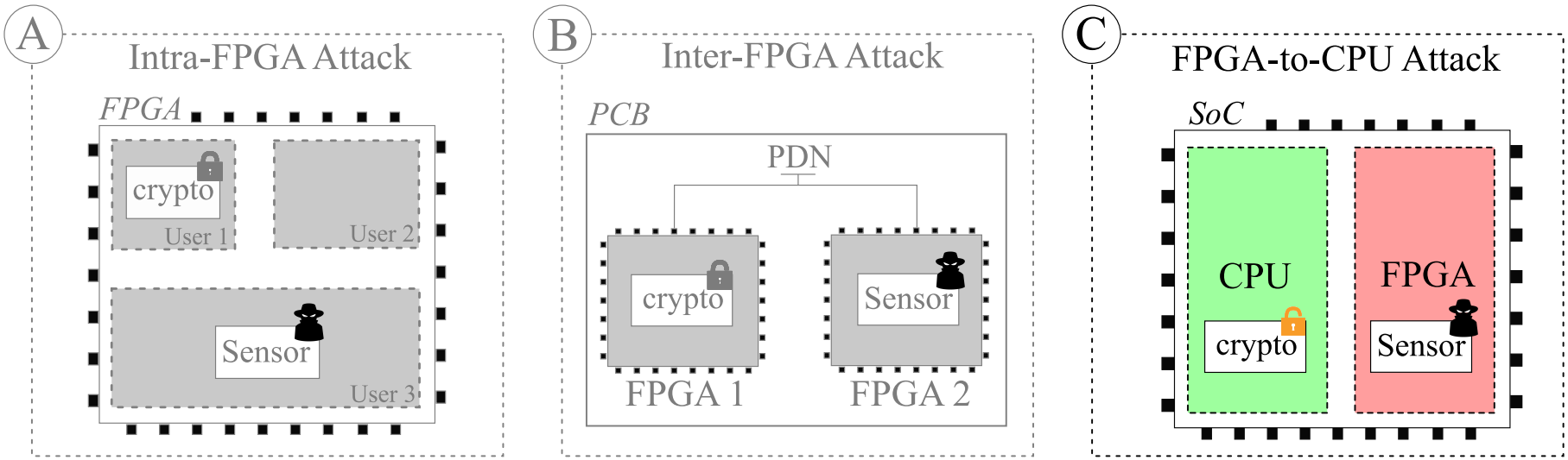

- Already proved:
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  - **SPA** attack on **self-written** software RSA using **ROs**.
- Our Goal:
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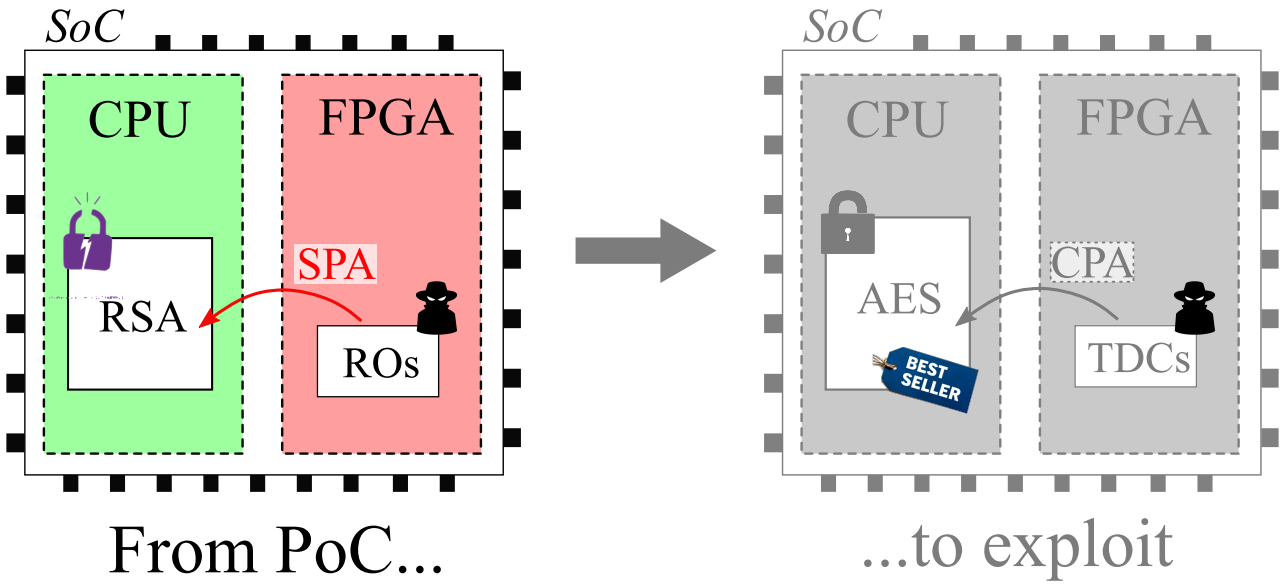

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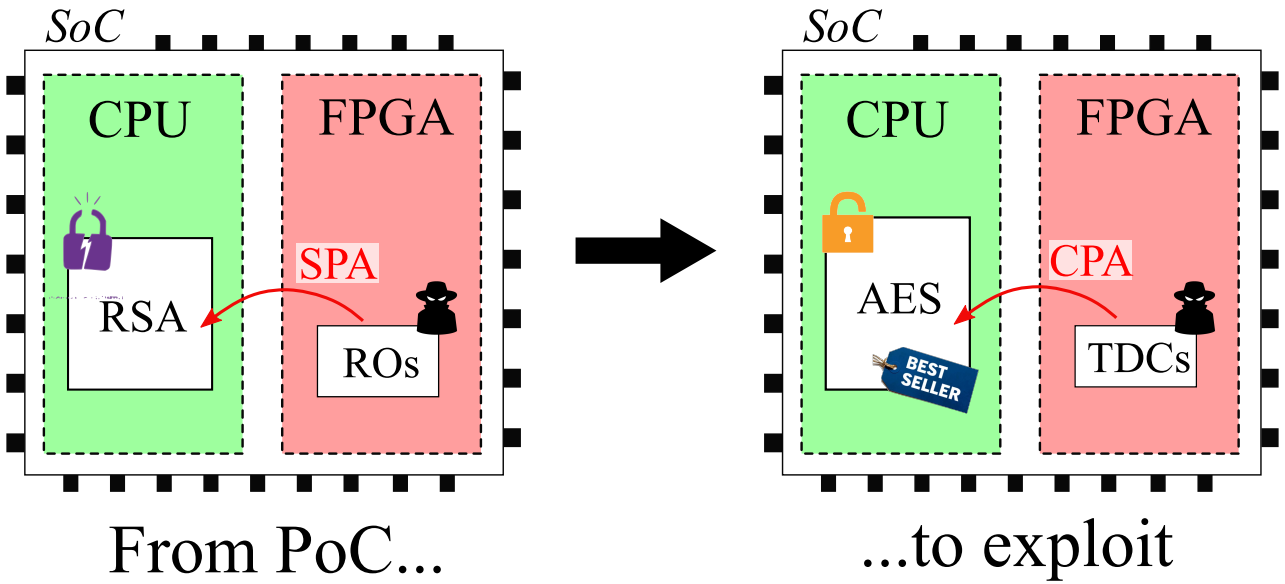

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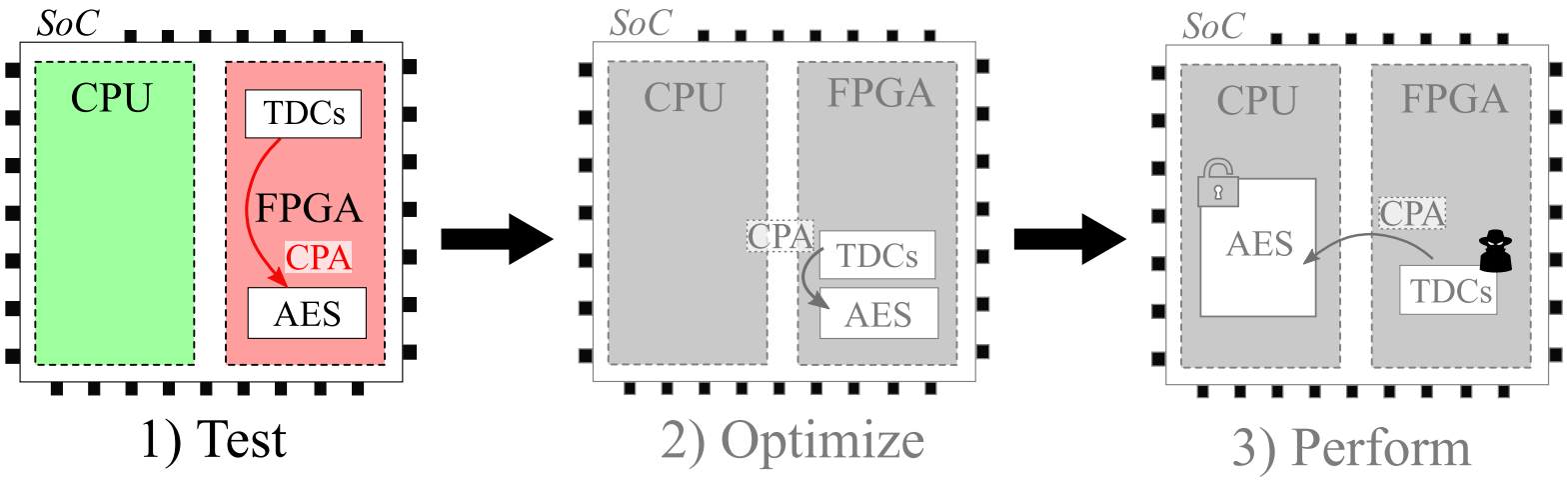

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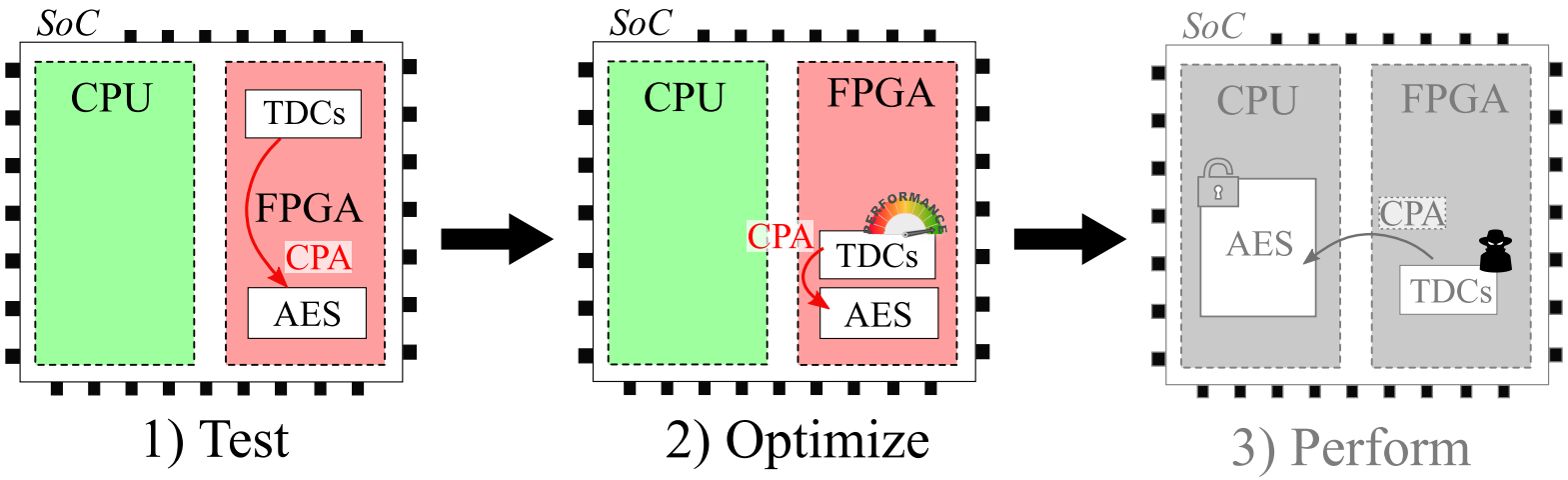

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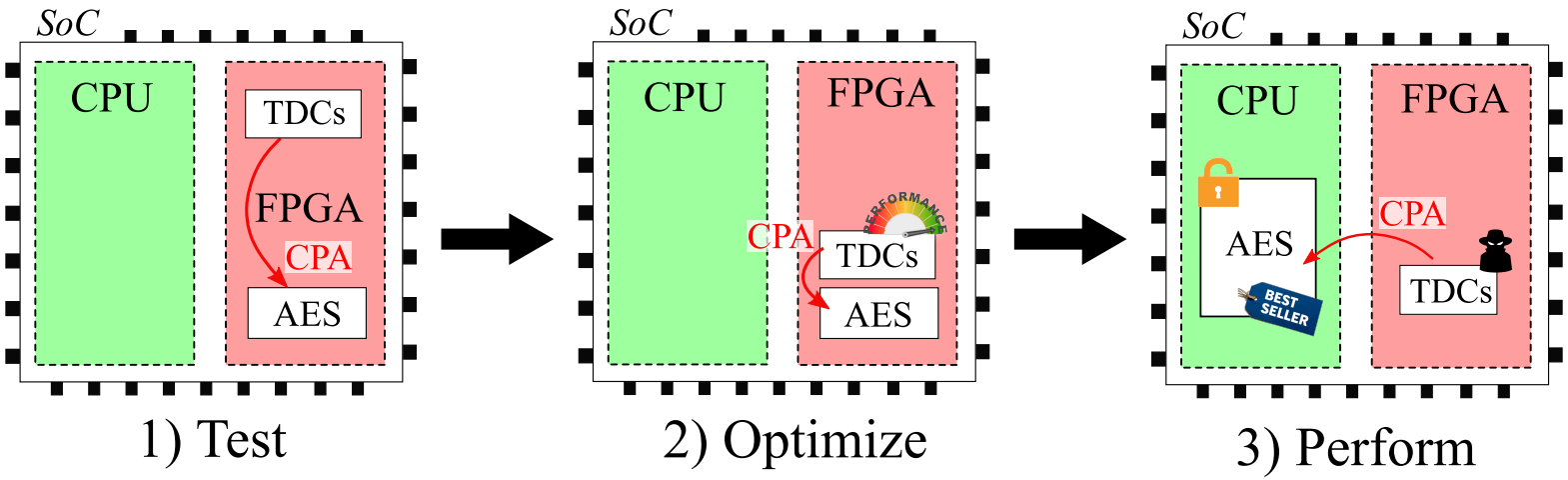
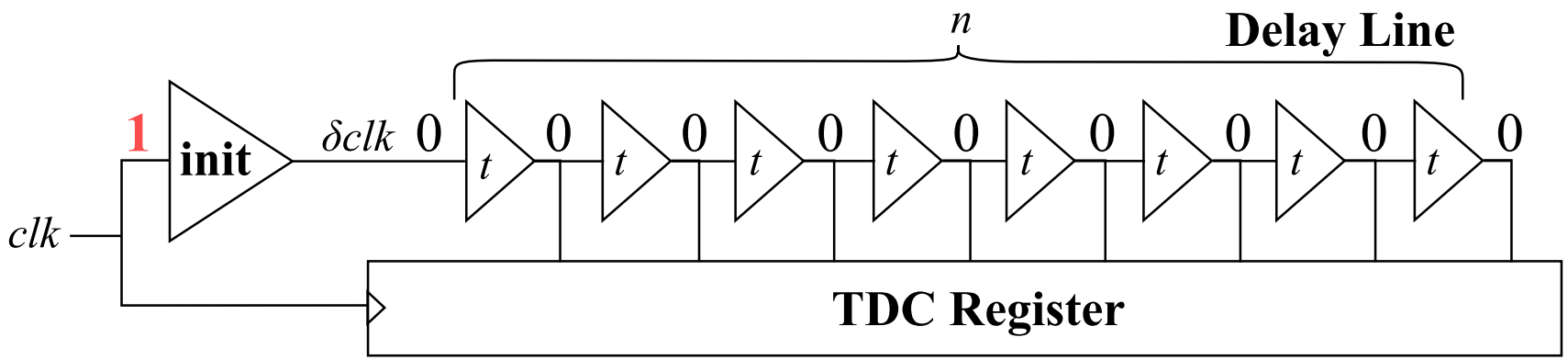


1. **Hardware** AES encryption key retrieval.
2. FPGA-based SCA **Optimization**.
3. **Software** AES encryption key retrieval.

- Power supply fluctuations ⇒ Propagation delay variations.
- Time-To-Digital converter basics:
  - A *clk* **signal** propagates through a **delay line**.
  - A **register** periodically captures the **delay line** state.



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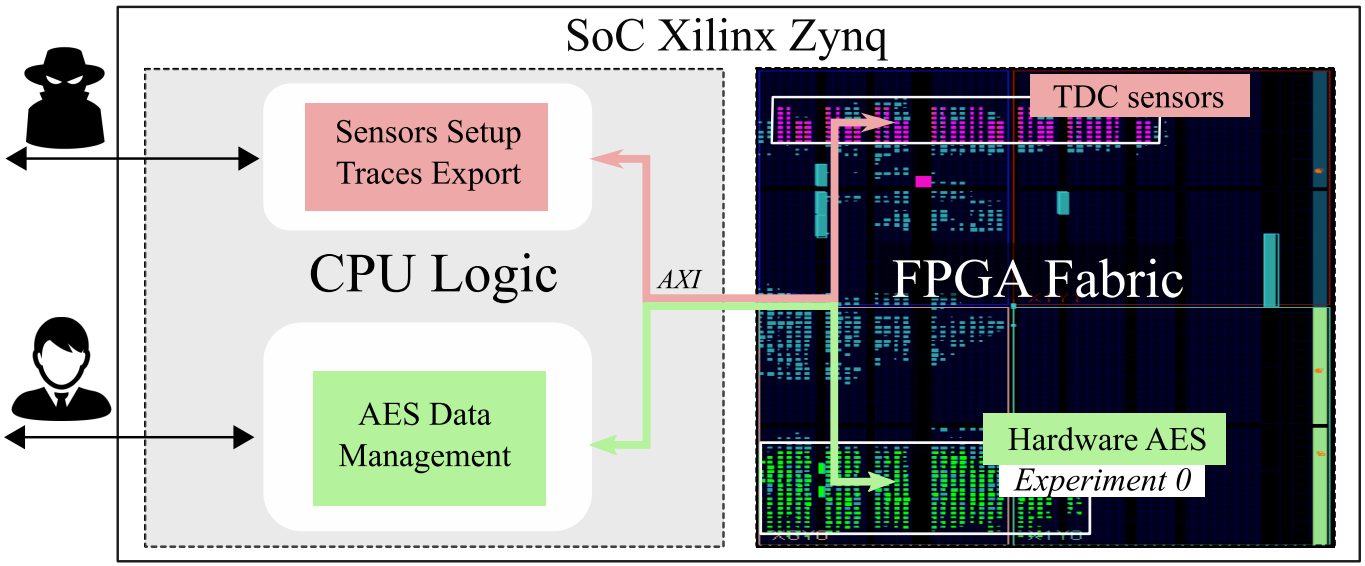
  - FPGA (Xilinx Artix-7) - TDC sensors and AES algorithm
  - CPU (ARM Cortex-A9) - Traces export and AES management



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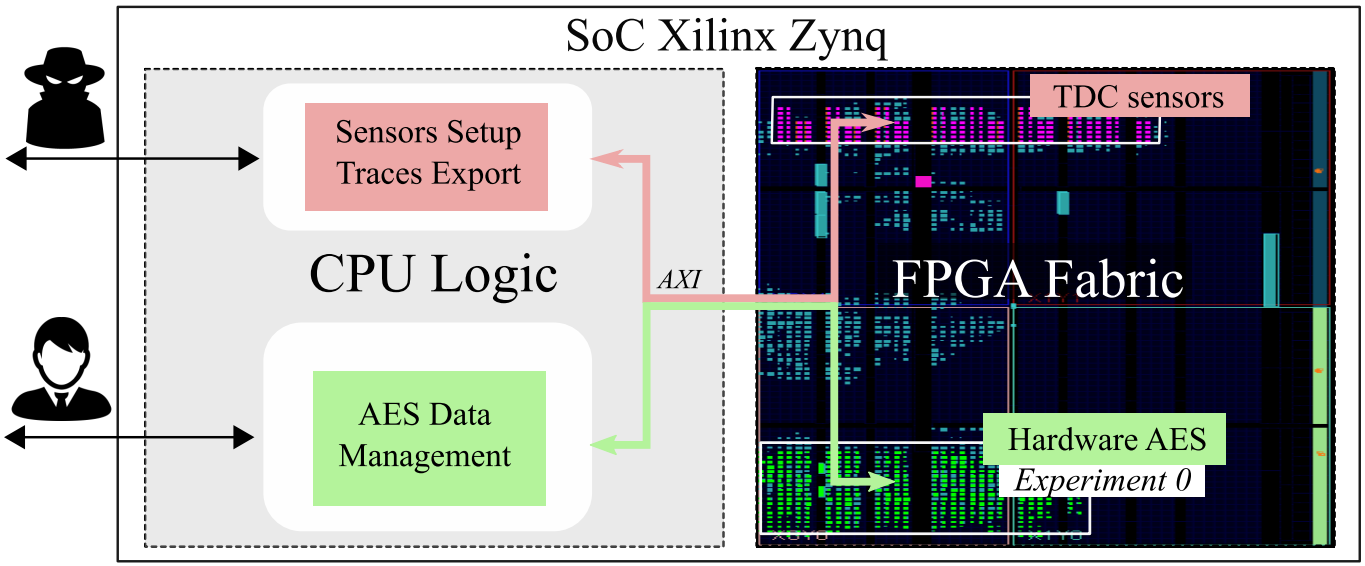
  - TDCs placed horizontally far away from AES => worst case scenario



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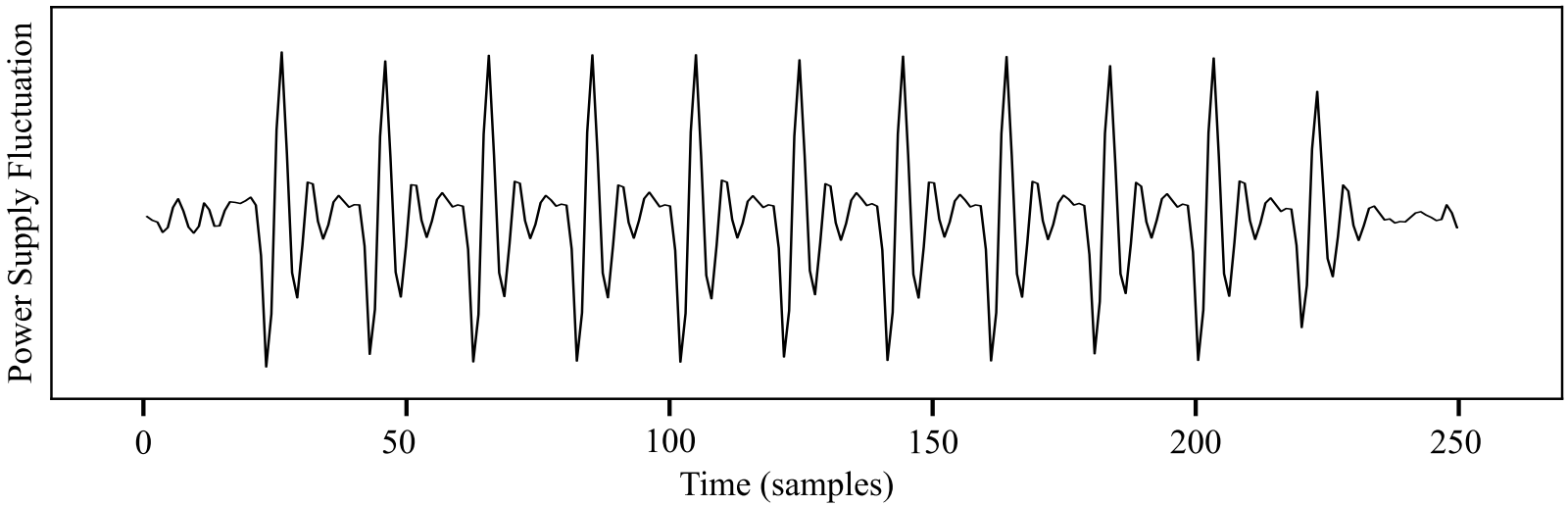

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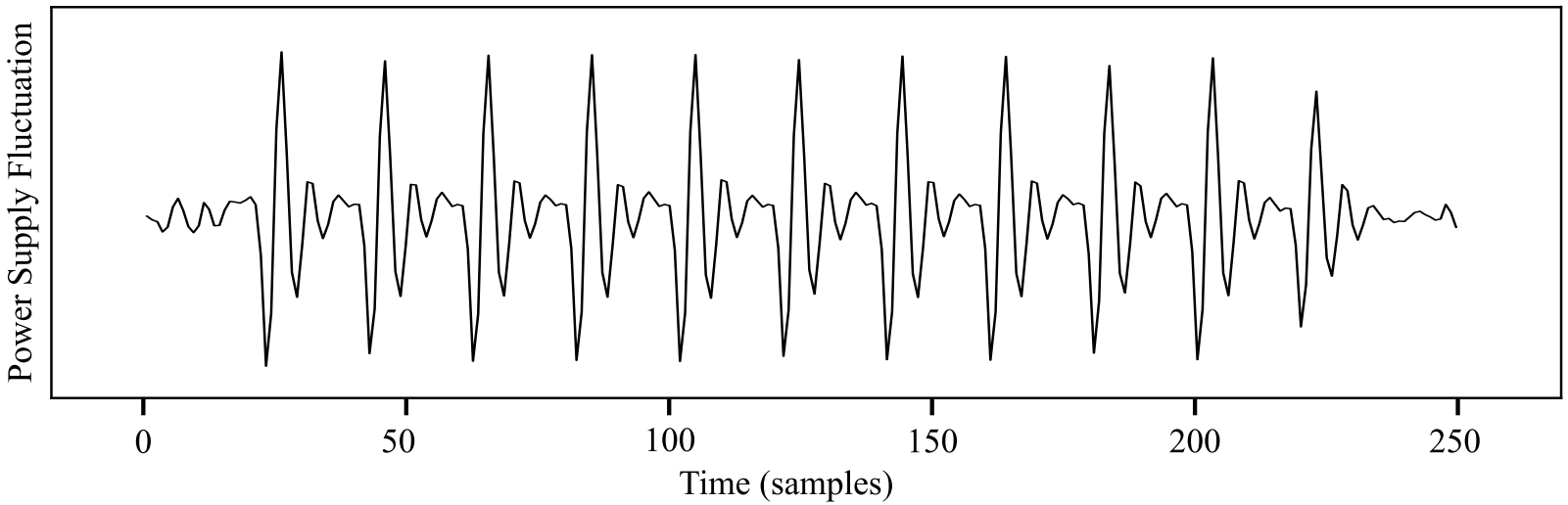

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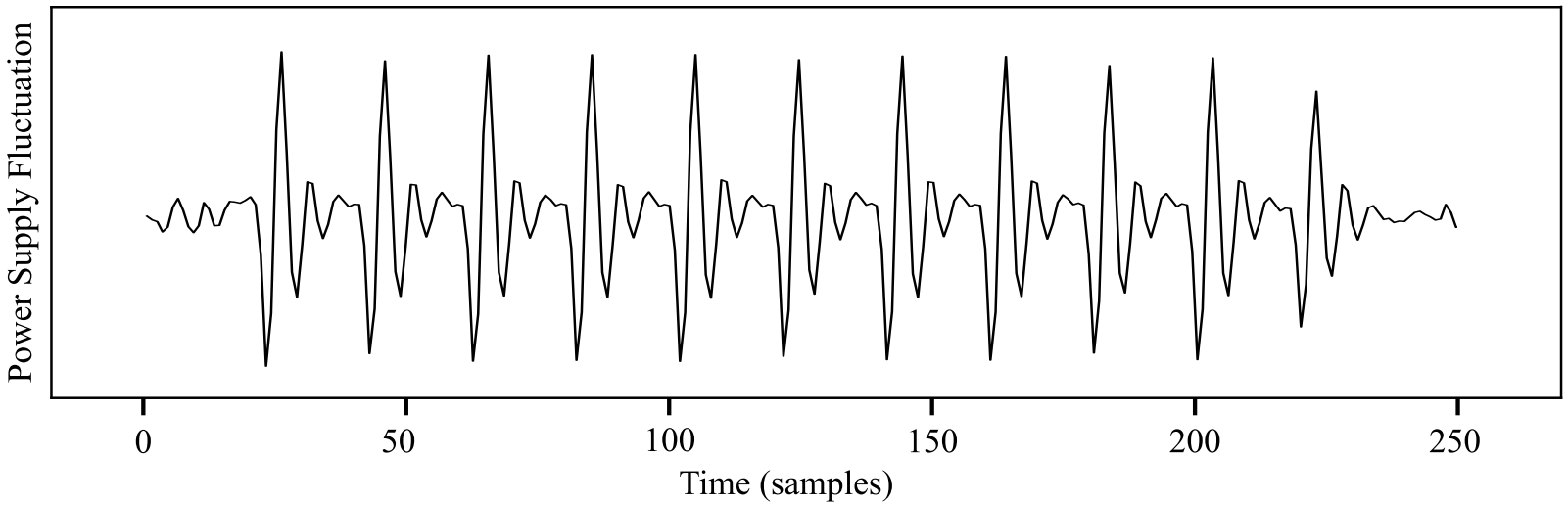

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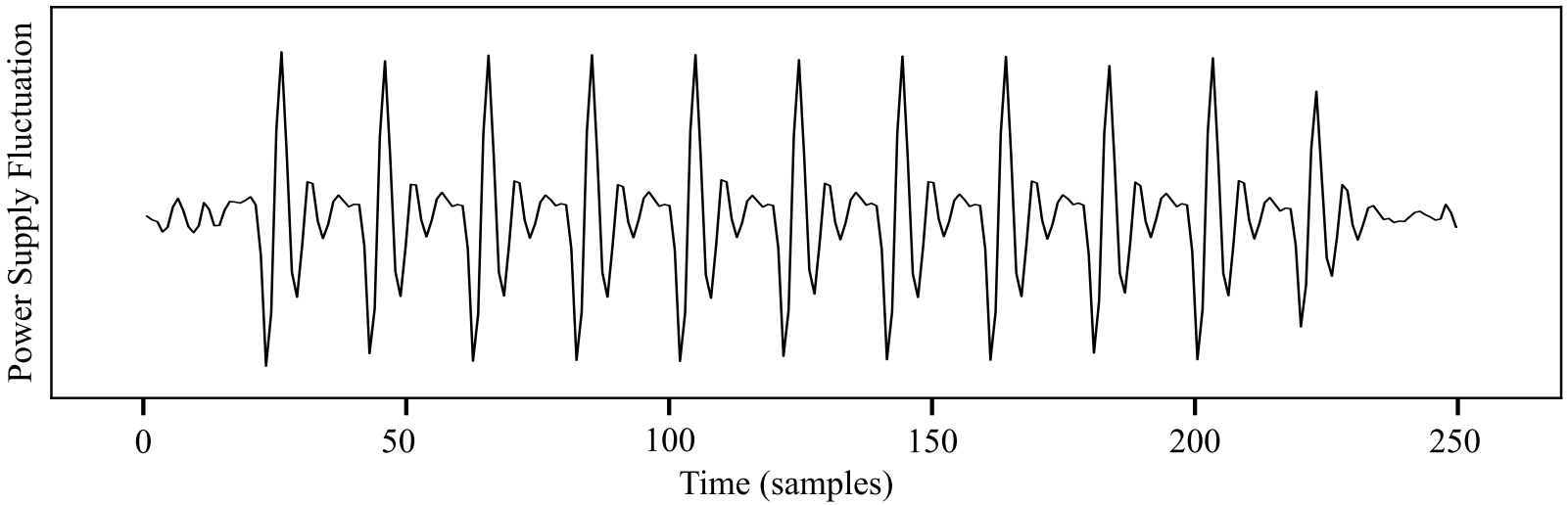

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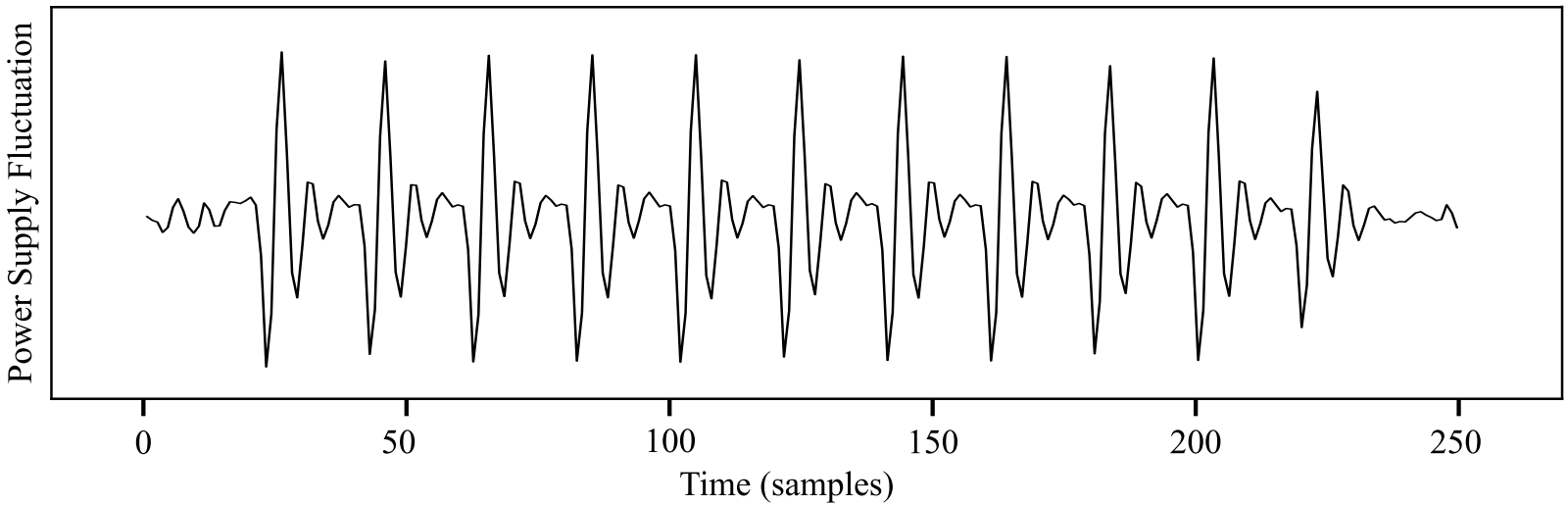

- Results: number of traces required to infer an AES key byte: **4,483**.

1. **Hardware** AES encryption key retrieval.
2. FPGA-based SCA **Optimization**.
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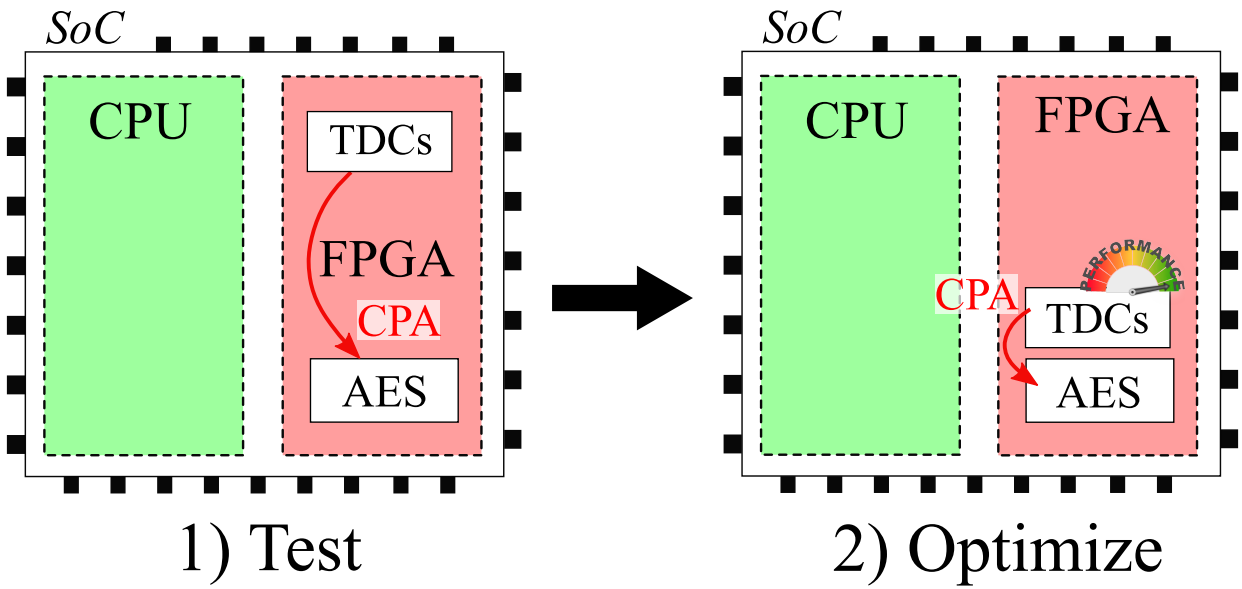
- Several levers:
  - Placement: TDCs **proximity** to the target.
  - Performance: TDCs **structure** modifications.



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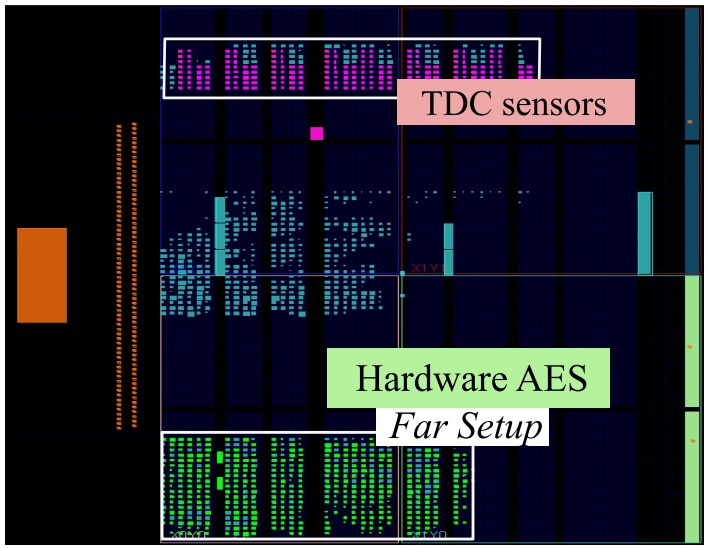

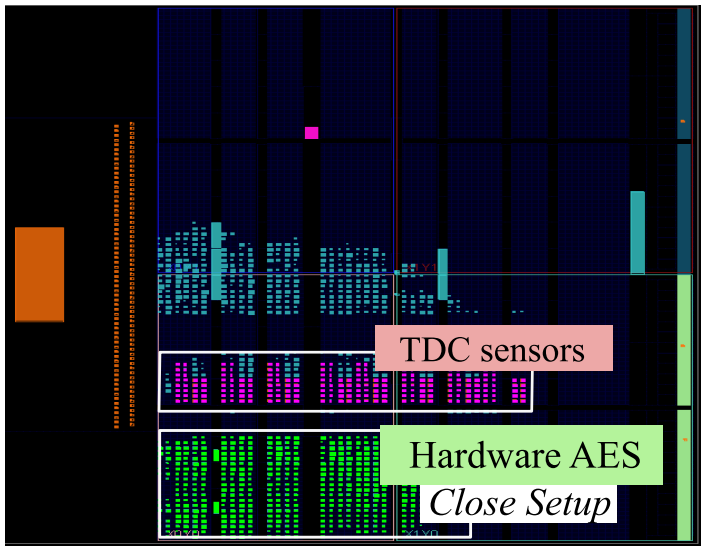

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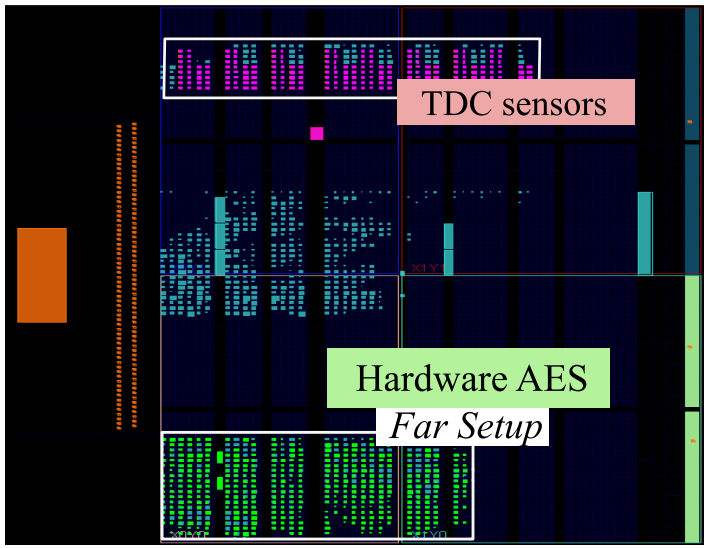

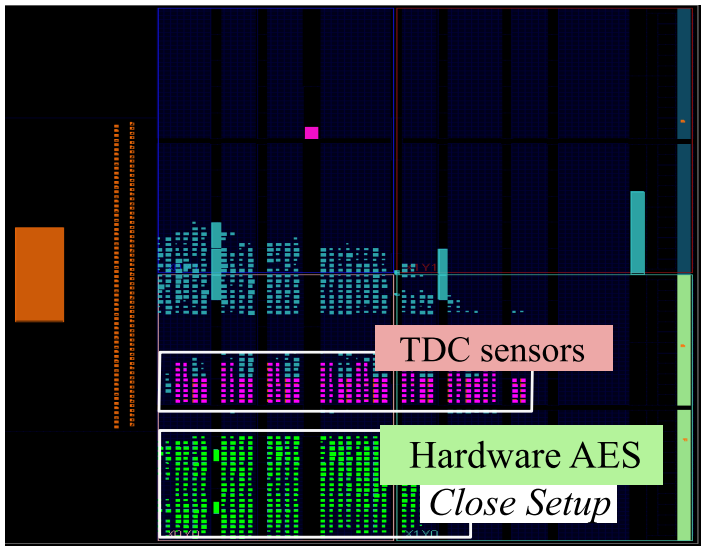

- Results: CPA traces required drops from 4,483 to **3,440**.

- Fixed (classic) **init** delay:
  - Add 180° phase shift to form δclk signal.
  - Integrates voltage fluctuations during a **half** *clk* period.
- Reconfigurable (new) **init** delay:
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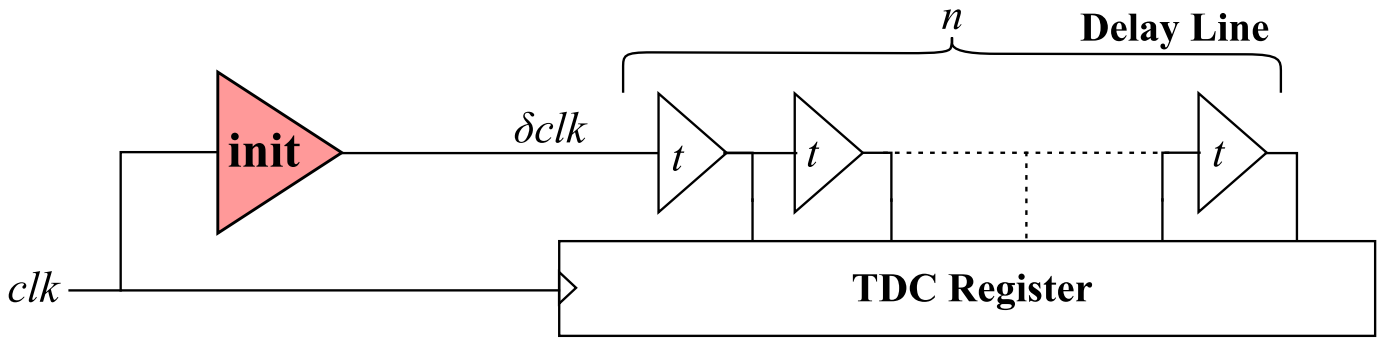

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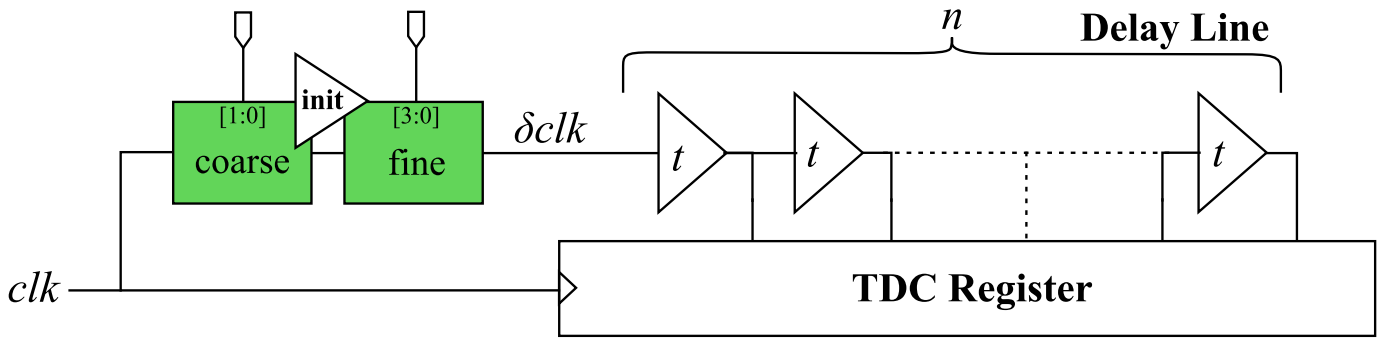

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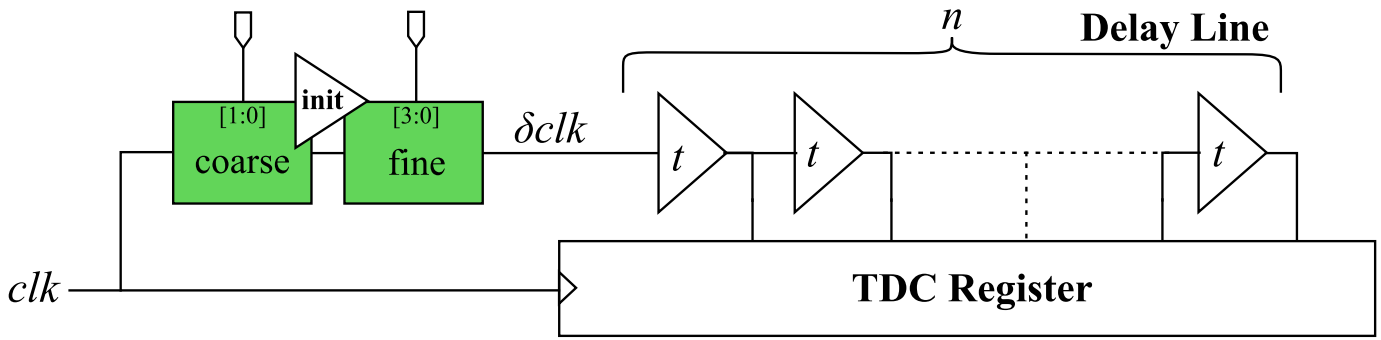

Reconfigurable *init* Delay

Results: CPA traces required **drops** from 3,440 to **1,381**.

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TDC Calibration	Average number of Traces	Optimization Factor
No	4,483	/
Placement	3,440	1,30
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- TDCs calibration is **substantial** for the following CPU attacks.
  - Low CPU-to-FPGA side-channel leakage.
  - CPU frequency @666MHz >> TDC frequency @200MHz.

1. **Hardware** AES encryption key retrieval.
2. FPGA-based SCA **Optimization**.
3. **Software** AES encryption key retrieval.

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  - Tiny AES 128 - **8 bit** data-path.
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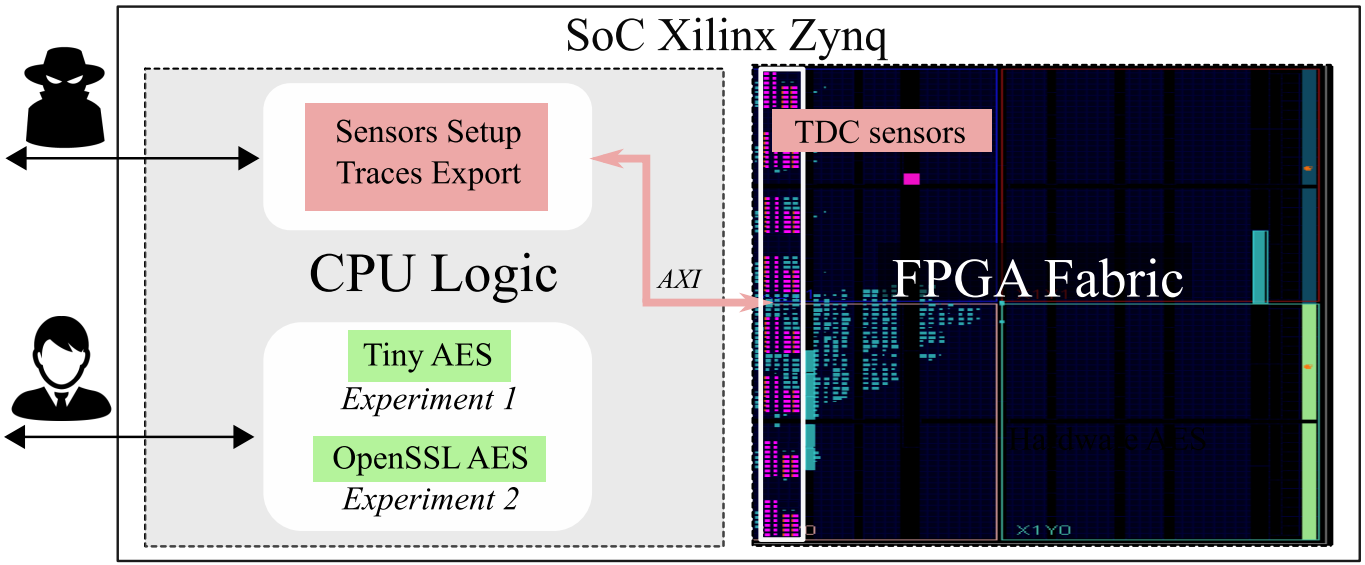
- Experimental setup:
  - 8 TDCs **placed vertically** on FPGA left part => make sense according to the implemented view.



- Small and portable implementation of the AES written in C.
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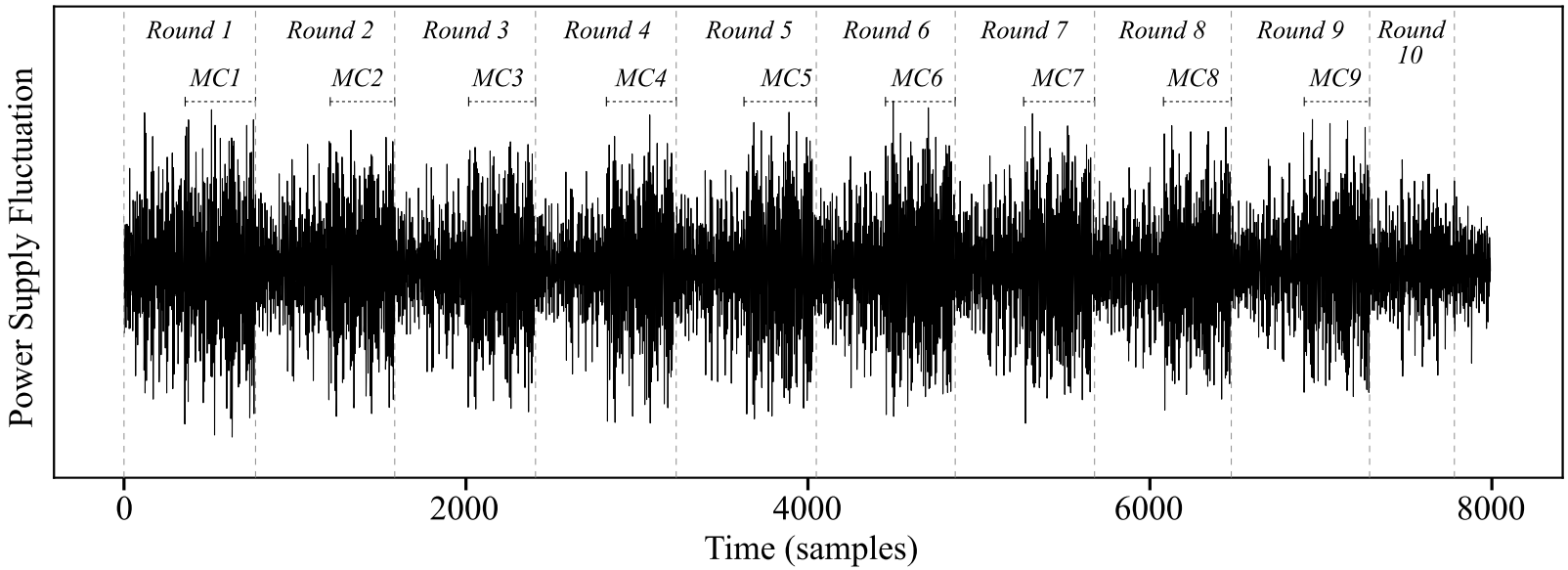

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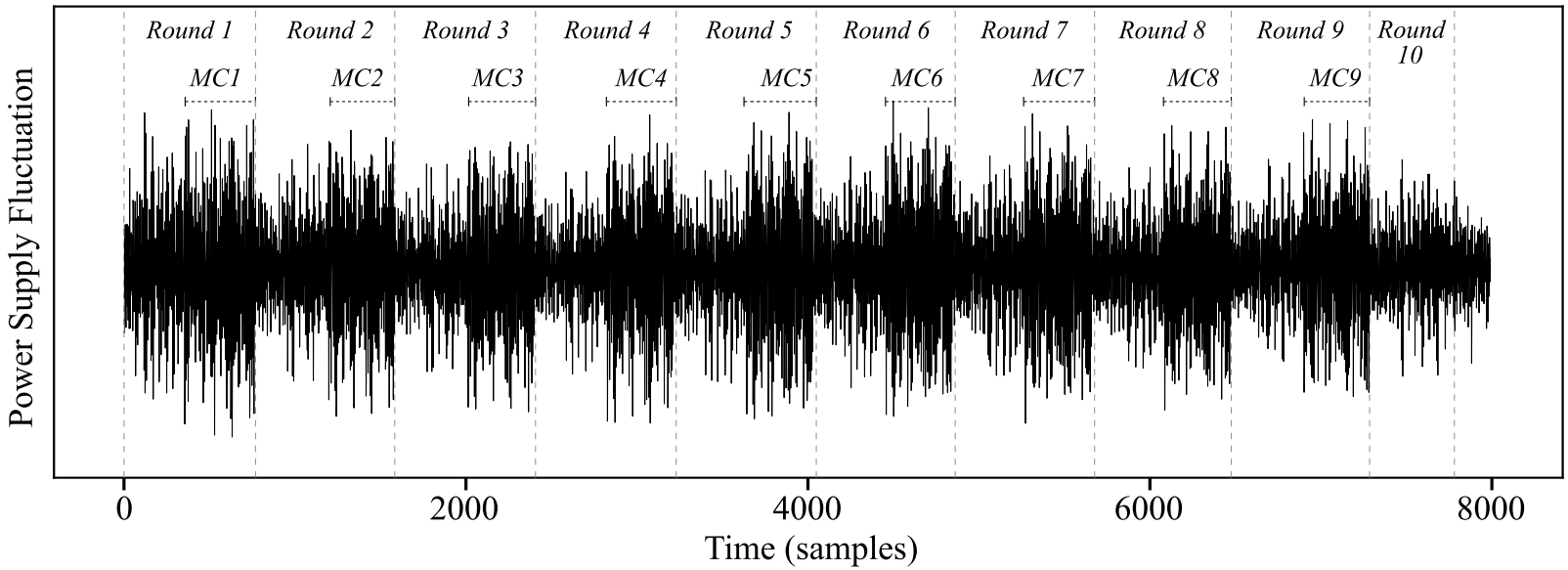

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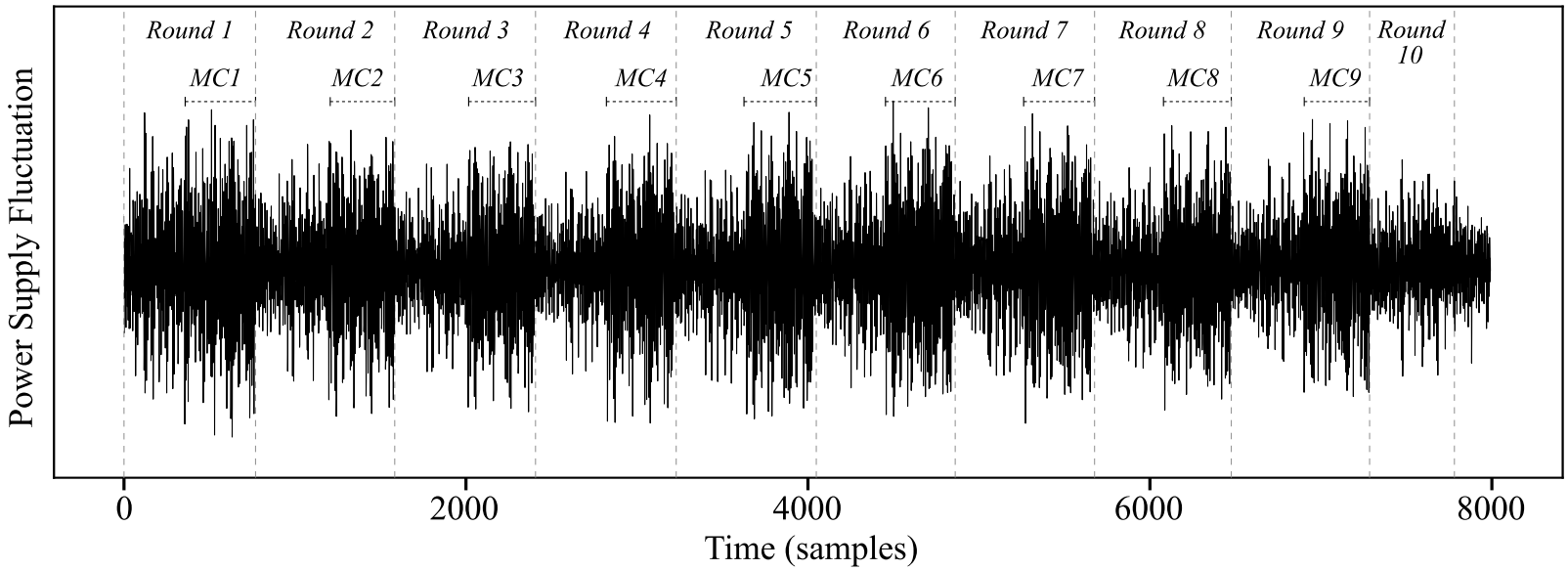

- **Number** of traces required to infer an AES key byte: **111,758**.

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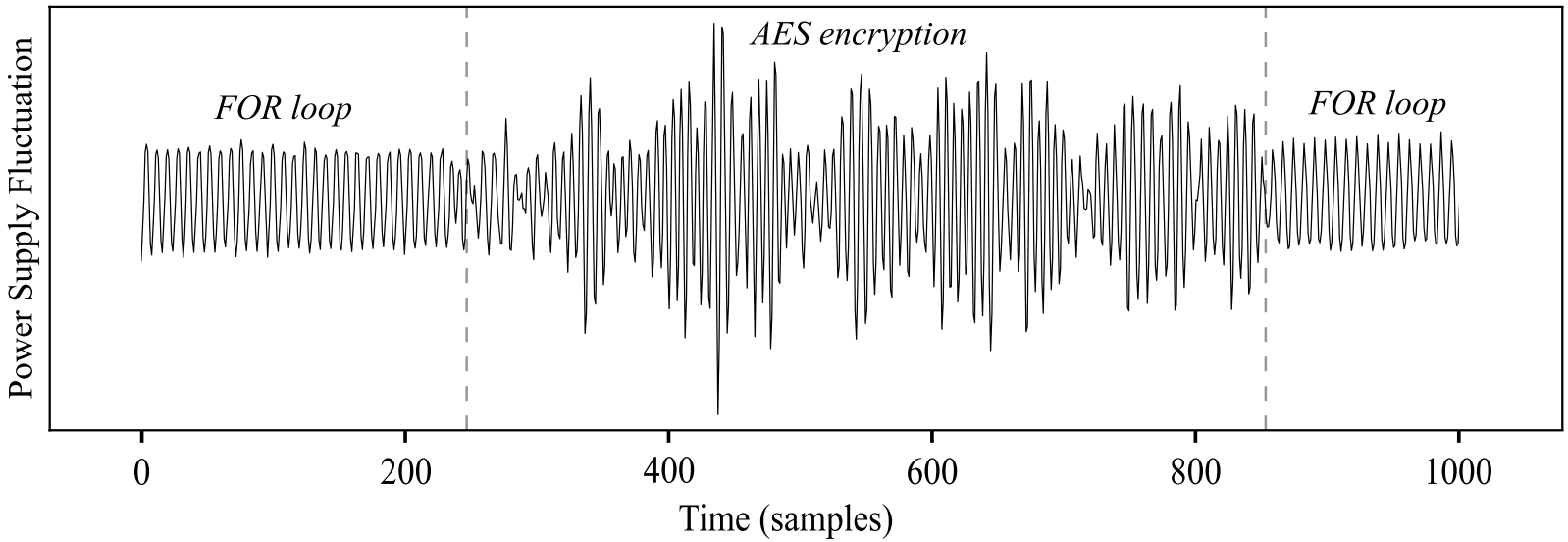

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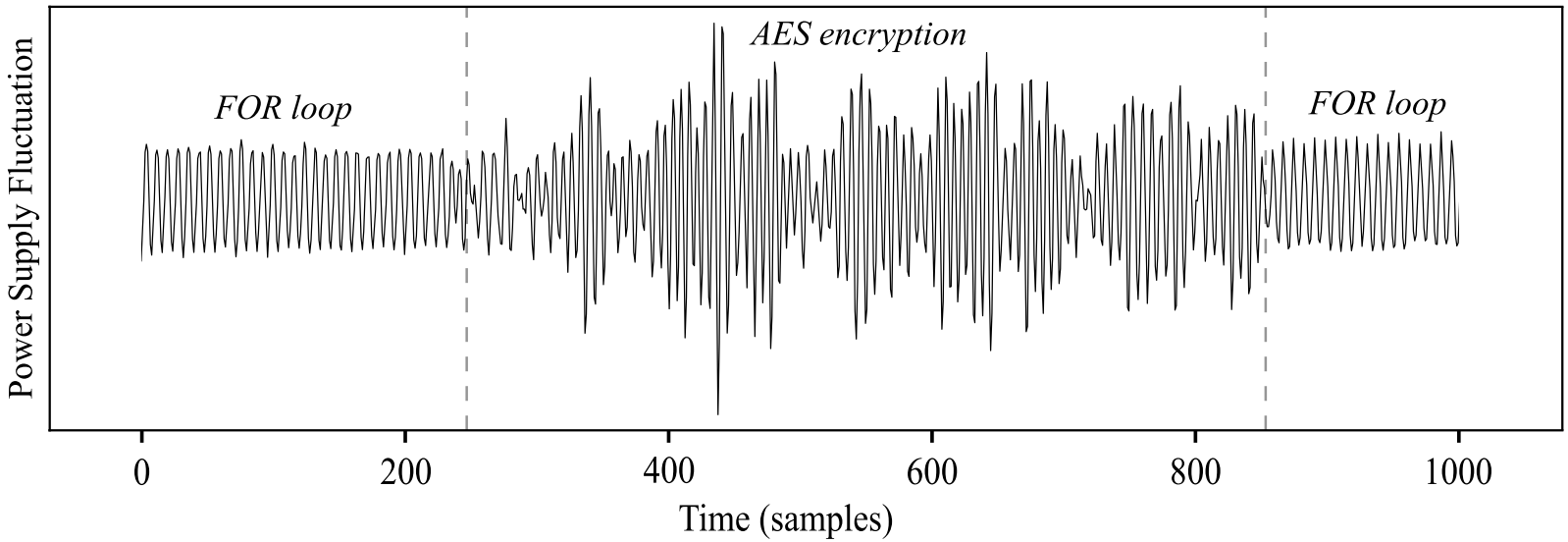

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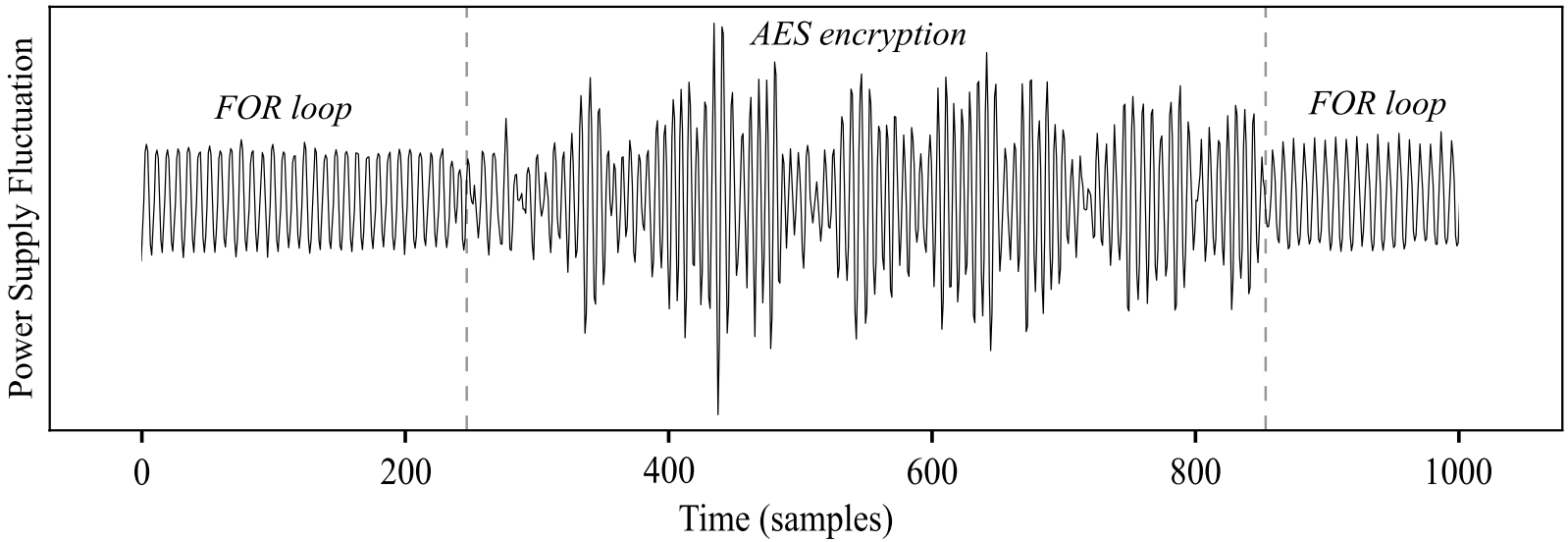

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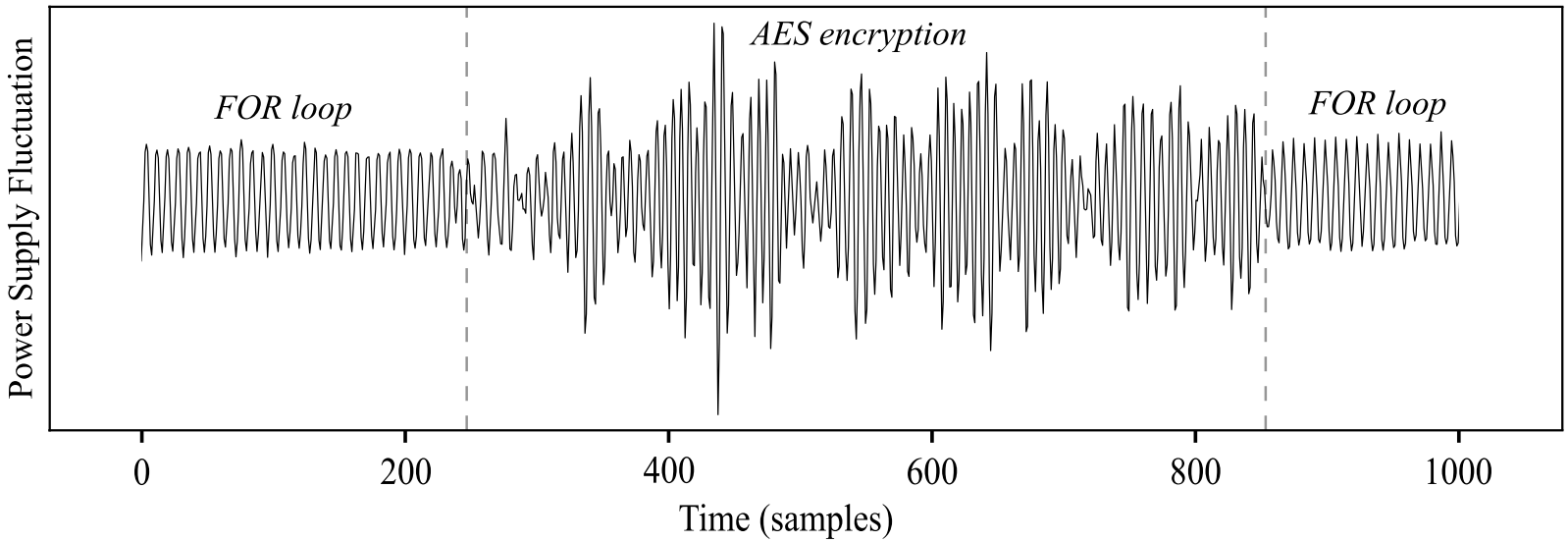

- **Number** of traces required to infer an AES key byte: **127,558**.

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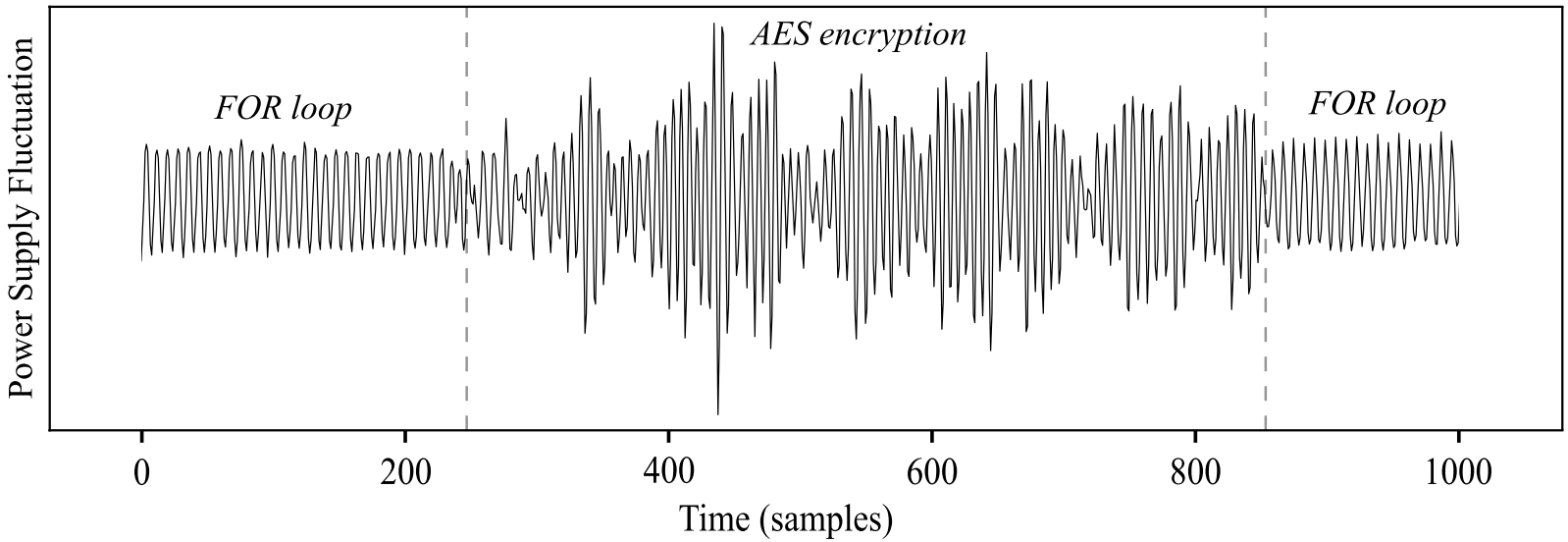
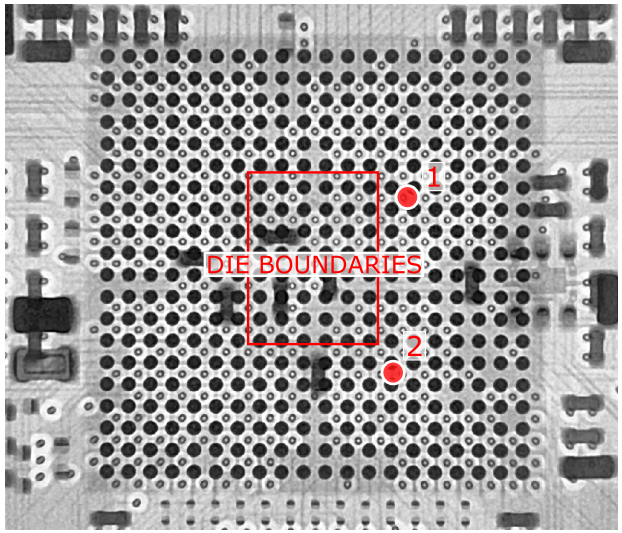
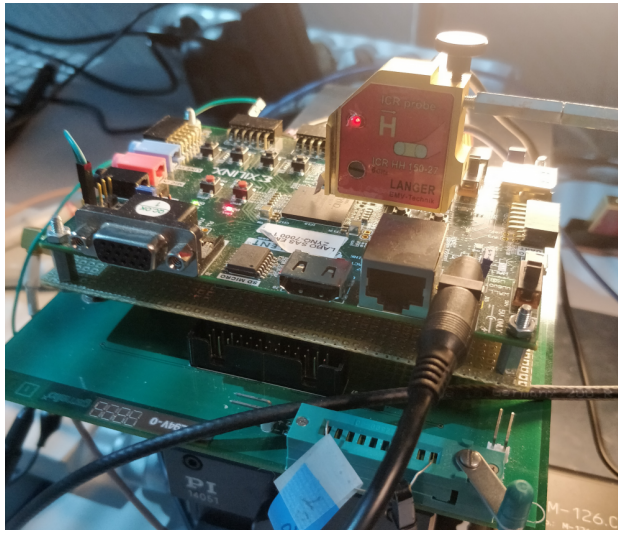


- **Number** of traces required to infer an AES key byte: **127,558**.
- Improved results with T-table model: **87,422** traces.

- Goal: **challenge** TDC results regarding **classical SCA**.
- Experimental Setup:
  - Probe: Langer ICR HH 150
  - Oscilloscope Sampling Rate: 5 GS/s





- Goal: **challenge** TDC results regarding **classical SCA**.
- Experimental Setup:
  - Probe: Langer ICR HH 150
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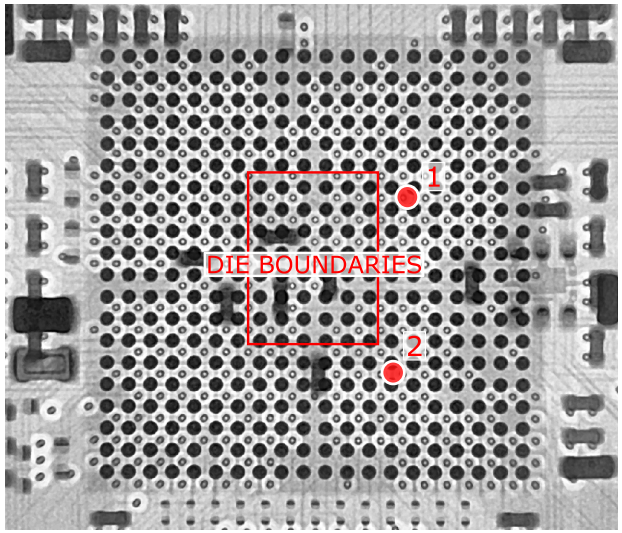
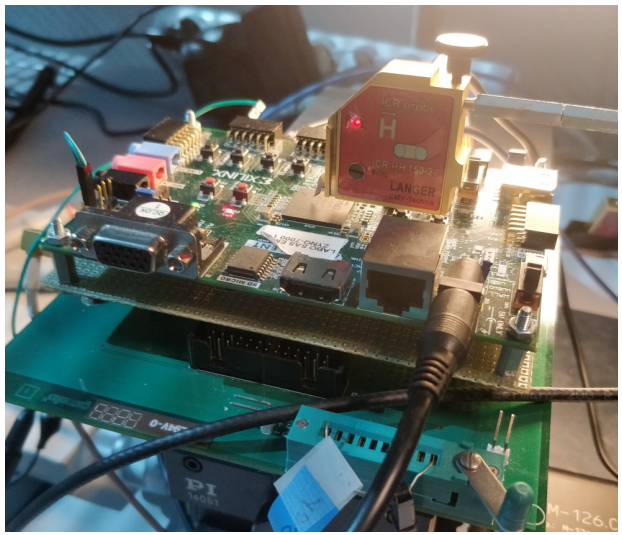
- Two hotspots:
  1. Best results for hardware AES algorithms. (**FPGA**)
  2. Best results for software AES algorithms. (**CPU**)





- CEMA conducted against **each AES studied**.
  - Osc sampling rate (5 GS/s) >> TDC sampling rate (200 MS/s).
  - Osc resolution >> TDC resolution

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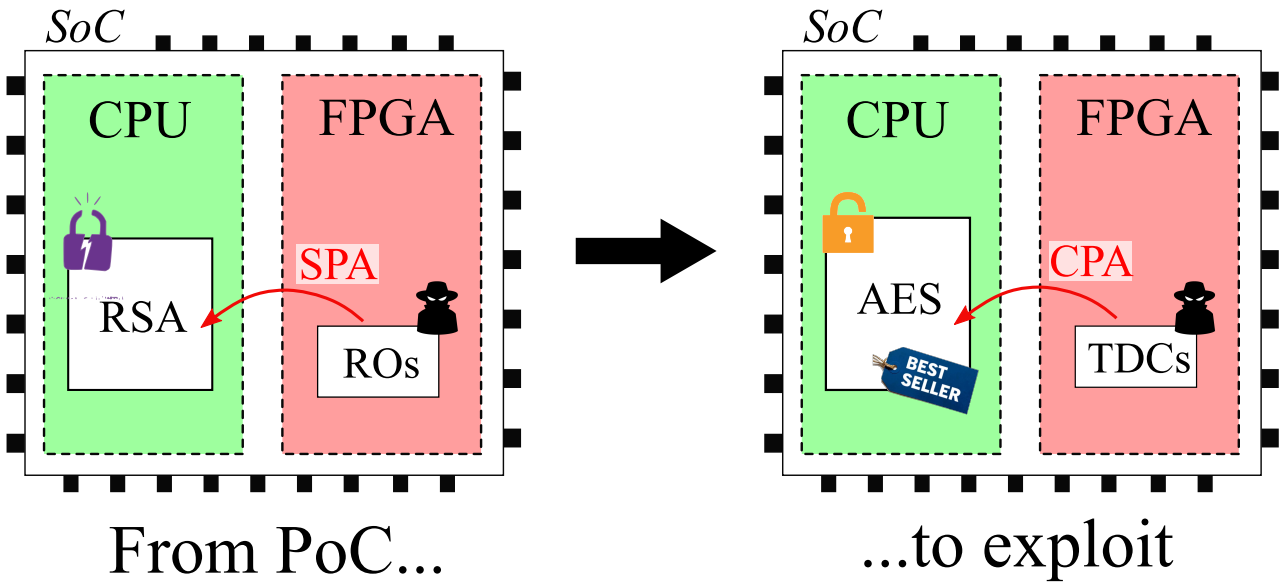
- TDCs provide similar results to local side-channel:
  - Side-channel leakage behaviour.
  - TDC calibration (position, delay).

- **FPGA-to-CPU statistical SCA attacks are practicable**.



- To do list:
  - TDC in-depth study (shape, number, chip...)
  - TDC against side-channel countermeasures (shuffling, masking, random delays, jitter, etc).

Thank you! Questions?

joseph.gravellier@emse.fr